L6711

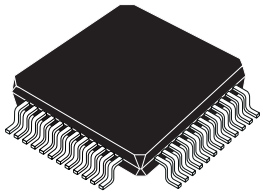
3 Phase controller with dynamic VID and selectable DACs

Features

- 2A integrated gate drivers
- Fully differential current reading across inductor or LS MOSFET
- 0.5% Output voltage accuracy
- 6 bit programmable output from 0.8185V to 1.5810V in 12.5mV steps
- 5 bit programmable output from 0.800V to 1.550V in 25mV steps
- Dynamic VID management
- Adjustable reference voltage offset
- 3% active current sharing accuracy
- Digital 2048 step soft-start
- Programmable over voltage protection
- Integrated temperature sensor
- Constant over current protection
- Oscillator internally fixed at 150kHz (450kHz ripple) externally adjustable
- Output enable
- Integrated remote sense buffer
- TQFP48 7x7 Package with exposed pad

Applications

- High current VRM/VRD for desktop / Server / Workstation CPUs
- High density DC/DC Converters



TQFP48 (Exposed Pad)

Description

The device implements a three phase step-down controller with a 120° phase-shift between each phase with integrated high current drivers in a compact 7x7mm body package with exposed pad.

The device embeds selectable DAC: the output voltage ranges from 0.8185V to 1.5810V with 12.5mV steps (VID_SEL = OPEN) or from 0.800V to 1.550V with 25mV steps (VID_SEL = GND; VID5 drives an optional +25mV offset) managing dynamic VID with 0.5% accuracy over line and temp variations. Additional programmable offset can be added to the voltage reference with a single external resistor.

The device assures a fast protection against load over current and load over/under voltage. An internal crowbar is provided turning on the low side mosfet if an over-voltage is detected.

In case of over-current, the system works in Constant Current mode until UVP.

Selectable current reading adds flexibility in system design.

Order codes

Part Number	Package	Packing
L6711	TQFP48	Tube
L6711TR	TQFP48	Tape & Reel

Contents

1 Typical application circuit and block diagram

1.1 Application circuit

Figure 1. Typical application circuit for LS MOSFET current sense

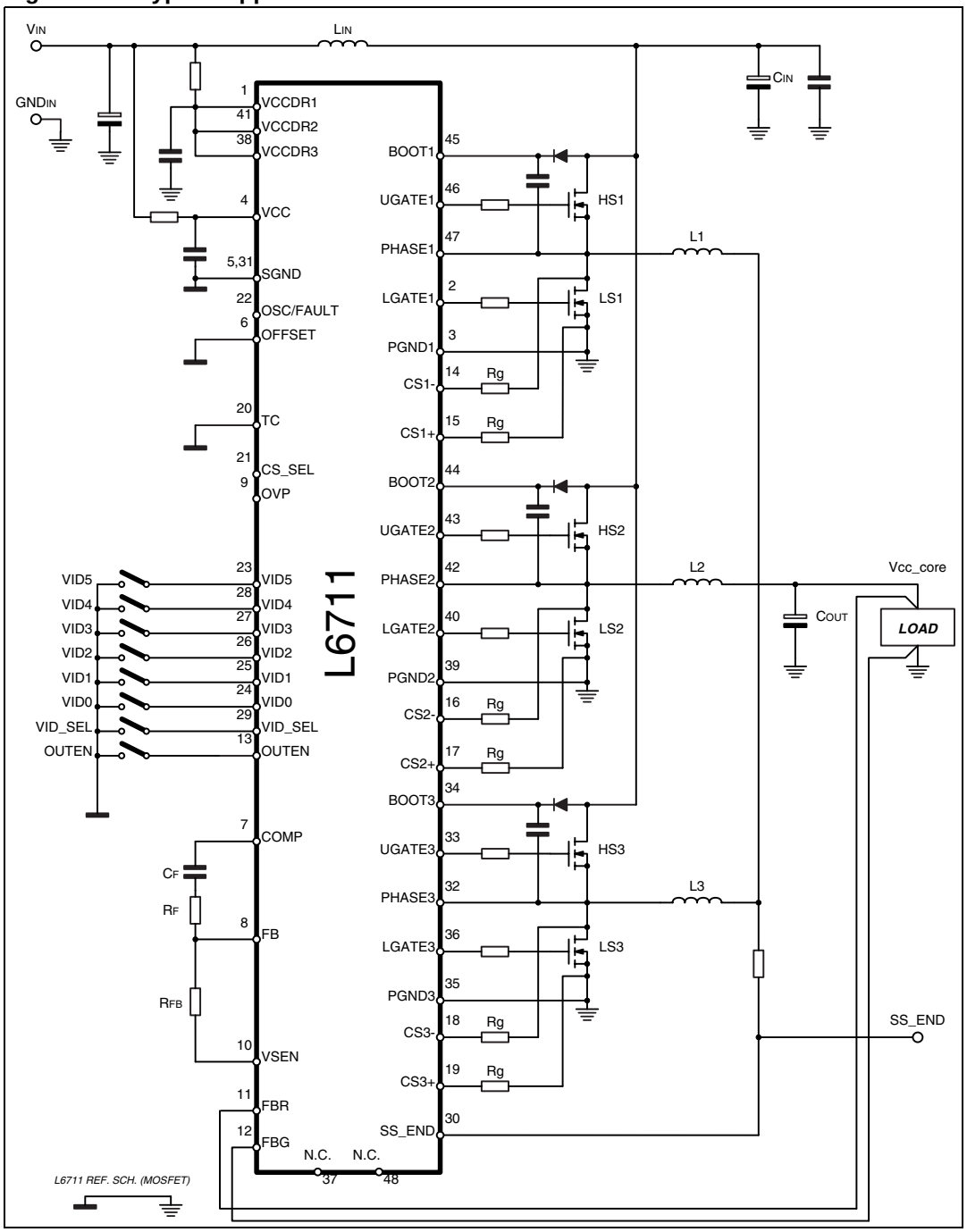
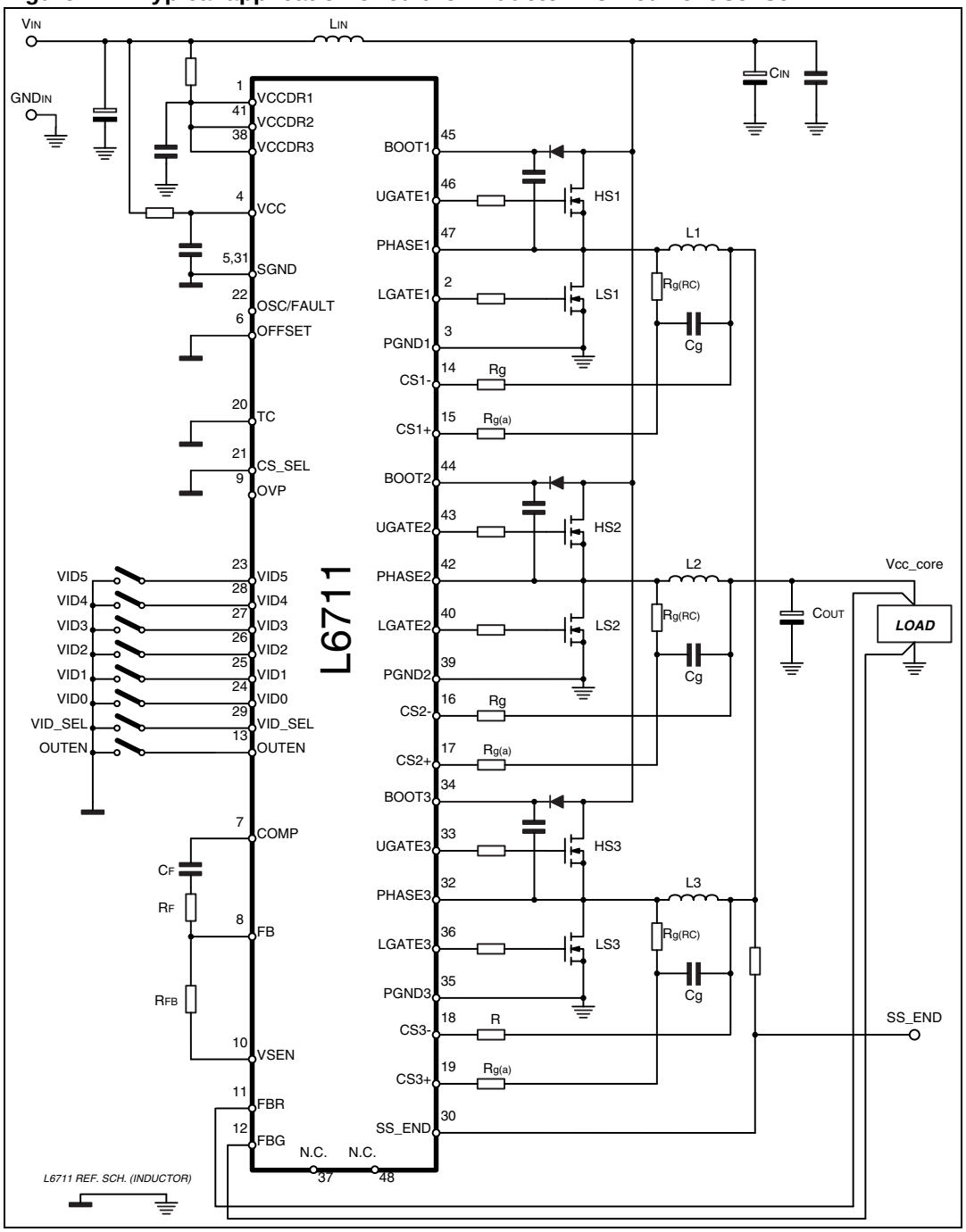
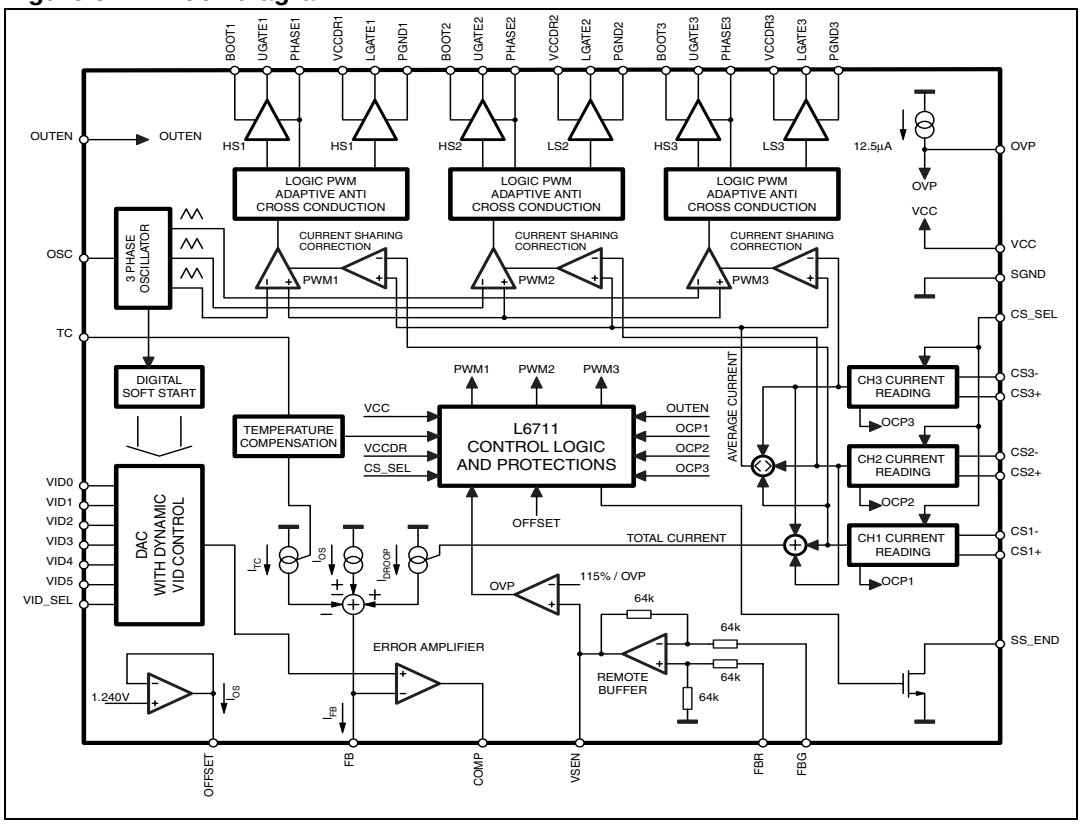


Figure 2. Typical application circuit for inductor DCR current sense



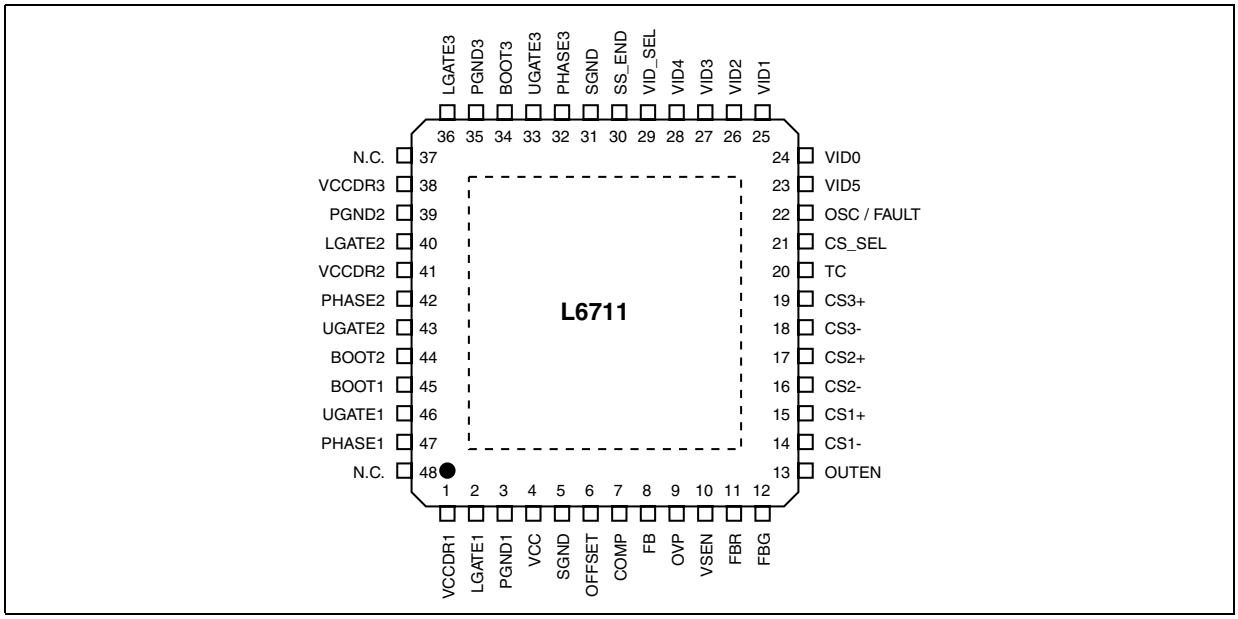
1.2 Block diagram

Figure 3. Block diagram



2 Pins description and connection diagrams

Figure 4. Pins connection (top view)



2.1 Pin descriptions

Table 1. Pins description

N°	Name	Description
1	VCCDR1	Channel 1 LS driver supply: it can be varied from 5V to 12V buses. It must be connected together with other VCCDRx pins. Filter locally with at least 1µF ceramic cap vs. PGND1.
2	LGATE1	Channel 1 LS driver output. A little series resistor helps in reducing device-dissipated power.
3	PGND1	Channel 1 LS driver return path. Connect to Power Ground Plane.
4	VCC	Device supply voltage. The operative supply voltage is 12V ±15%. Filter with 1µF capacitor (Typ.) vs. SGND.
5	SGND	All the internal references are referred to this pin. Connect it to the PCB signal ground.
6	OFFSET	Offset programming pin, internally fixed at 1.240V. Short to SGND to disable the offset generation or connect through a resistor R_{OFFSET} to SGND to program an offset (positive or negative, depending on TC status) to the regulated output voltage as reported in the relative section.
7	COMP	This pin is connected to the error amplifier output and is used to compensate the control feedback loop.

Table 1. Pins description (continued)

N°	Name	Description
8	FB	This pin is connected to the error amplifier inverting input and is used to compensate the voltage control feedback loop. Connecting a resistor between this pin and VSEN pin allows programming the droop effect.
9	OVP	Over Voltage protection setup pin: it allows programming the OVP intervention. Internally pulled-up to 5V, it sources a constant 12.5µA current. Leaving the pin floating the OVP threshold is set to 115% (Typ.) of the programmed voltage Connecting a resistor R_{OVP} to SGND, it sets the OVP threshold to a fixed programmable voltage (see relevant section for further details). Filter with 10nF vs. SGND in this case.
10	VSEN	Manages Over&Under-voltage conditions. It is internally connected with the output of the Remote Sense Buffer for Remote Sense of the regulated voltage. If no Remote Sense is implemented, connect it directly to the regulated voltage in order to manage OVP and UVP.
11	FBR	Remote sense buffer non-inverting input. It has to be connected to the positive side of the load to perform a remote sense.
12	FBG	Remote sense buffer inverting input. It has to be connected to the negative side of the load to perform a remote sense.
13	OUTEN	Output Enable pin; internally 3V pulled-up, it can be pulled-up with a resistor up to 3.3V. If forced to a voltage lower than 0.3V, the device stops operation with all mosfets OFF: all the protections are disabled in this condition except pre-OVP. Cycle this pin to recover latch from protections; filter with 1nF (Typ.) capacitor vs. SGND.
14	CS1-	Channel 1 Current Sense Negative Input pin. It must be connected through an Rg resistor to the LS mosfet drain (or to the LS-side of the sense resistor placed in series to the LS mosfet) if LS mosfet sense is performed (CS_SEL=OPEN). Otherwise (CS_SEL=SGND), it must be connected to the output-side of the output inductor (or the output-side of the sense resistor used and placed between the channel 1 inductor and the output of the converter) through Rg resistor. The net connecting the pin to the sense point must be routed as close as possible to the CS1+ net in order to couple in common mode any picked-up noise.
15	CS1+	Channel 1 Current Sense Positive Input pin. It must be connected through an Rg resistor to the LS mosfet source (or to the GND-side of the sense resistor placed in series to the LS mosfet) if LS mosfet sense is performed (CS_SEL=OPEN). Otherwise (CS_SEL=SGND), it must be connected to the phase-side of the output inductor (or the inductor-side of the sense resistor used and placed between the channel 1 inductor and the output of the converter) through Rg resistor and an R-C network across the inductor. The net connecting the pin to the sense point must be routed as close as possible to the CS1- net in order to couple in common mode any picked-up noise.
16	CS2-	Channel 2 Current Sense Negative Input pin. It must be connected through an Rg resistor to the LS mosfet drain (or to the LS-side of the sense resistor placed in series to the LS mosfet) if LS mosfet sense is performed (CS_SEL=OPEN). Otherwise (CS_SEL=SGND), it must be connected to the output-side of the output inductor (or the output-side of the sense resistor used and placed between the channel 2 inductor and the output of the converter) through Rg resistor. The net connecting the pin to the sense point must be routed as close as possible to the CS2+ net in order to couple in common mode any picked-up noise.

Table 1. Pins description (continued)

N°	Name	Description
17	CS2+	Channel 2 Current Sense Positive Input pin. It must be connected through an Rg resistor to the LS mosfet source (or to the GND-side of the sense resistor placed in series to the LS mosfet) if LS mosfet sense is performed (CS_SEL=OPEN). Otherwise (CS_SEL=SGND), it must be connected to the phase-side of the output inductor (or the inductor-side of the sense resistor used and placed between the channel 2 inductor and the output of the converter) through Rg resistor and an R-C network across the inductor. The net connecting the pin to the sense point must be routed as close as possible to the CS2- net in order to couple in common mode any picked-up noise.
18	CS3-	Channel 3 Current Sense Negative Input pin. It must be connected through an Rg resistor to the LS mosfet drain (or to the LS-side of the sense resistor placed in series to the LS mosfet) if LS mosfet sense is performed (CS_SEL=OPEN). Otherwise (CS_SEL=SGND), it must be connected to the output-side of the output inductor (or the output-side of the sense resistor used and placed between the channel 3 inductor and the output of the converter) through Rg resistor. The net connecting the pin to the sense point must be routed as close as possible to the CS3+ net in order to couple in common mode any picked-up noise.
19	CS3+	Channel 3 Current Sense Positive Input pin. It must be connected through an Rg resistor to the LS mosfet source (or to the GND-side of the sense resistor placed in series to the LS mosfet) if LS mosfet sense is performed (CS_SEL=OPEN). Otherwise (CS_SEL=SGND), it must be connected to the phase-side of the output inductor (or the inductor-side of the sense resistor used and placed between the channel 3 inductor and the output of the converter) through Rg resistor and an R-C network across the inductor. The net connecting the pin to the sense point must be routed as close as possible to the CS3- net in order to couple in common mode any picked-up noise.
20	TC	Temperature Compensation pin. Connect through a resistor R_{TC} and filter with 10nF vs. SGND to program the temperature compensation effect. Short to SGND to disable the compensation effect.
21	CS_SEL	Current Reading Selection pin, internally 5V pulled-up. Leave floating to sense current across low-side mosfets or a sense resistor placed in series to the LS mosfet source. Maximum duty cycle is dynamically limited and Track&Hold is enabled to assure proper reading of the current. Short to SGND to read current across inductors or a sense resistor placed in series to the output inductors. No duty cycle limitation and no Track&Hold performed in this case.
22	OSC / FAULT	Oscillator pin. It allows programming the switching frequency of each channel: the equivalent switching frequency at the load side results in being tripled. Internally fixed at 1.24V, the frequency is varied proportionally to the current sunk (forced) from (into) the pin with an internal gain of 6kHz/µA (See relevant section for details). If the pin is not connected, the switching frequency is 150kHz for each channel (450kHz on the load). The pin is forced high (5V Typ.) when an Over/Under Voltage is detected; to recover from this condition, cycle VCC or the OUTEN pin.

Table 1. Pins description (continued)

N°	Name	Description
23, 24 to 28	VID5, VID0-4	Voltage IDentification pins. Internally pulled-up to 3V, connect to SGND to program a logic '0' while leave floating (as well as pull-up with a resistor up to 3.3V) to program a logic '1'. They are used to program the output voltage as specified in *Table 5* and *Table 6* together with VID_SEL and to set the OVP/UVP protection thresholds accordingly. See relevant section for details about DAC selection.
29	VID_SEL	VID_SELect pin. Through this pin it is possible to select the DAC table used for the regulation. Leave floating to use a VRD10.x compliant DAC (See *Table 1*) while short to SGND to use a VRM-Hammer compliant DAC (See *Table 3*). See relevant section for details about DAC selection.
30	SS_END	Soft start end signal. It is an open collector output, set free after finishing the soft start. Pull-up with a resistor to a voltage lower than 5V, if not used may be left floating.
31	SGND	All the internal references are referred to this pin. Connect it to the PCB signal ground.
32	PHASE3	Channel 3 HS driver return path. It must be connected to the HS3 mosfet source and provides the return path for the HS driver of channel 3.
33	UGATE3	Channel 3 HS driver output. A little series resistor helps in reducing device-dissipated power.
34	BOOT3	Channel 3 HS driver supply. This pin supplies the relative high side driver. Connect through a capacitor (100nF Typ.) to the PHASE3 pin and through a diode to VCC (cathode vs. boot).
35	PGND3	Channel 3 LS driver return path. Connect to Power Ground Plane.
36	LGATE3	Channel 3 LS driver output. A little series resistor helps in reducing device-dissipated power.
37	N.C.	Not internally connected.
38	VCCDR3	Channel 3 LS driver supply: it can be varied from 5V to 12V buses. It must be connected together with other VCCDRx pins. Filter locally with at least 1µF ceramic cap vs. PGND3.
39	PGND2	Channel 2 LS driver return path. Connect to Power Ground Plane.
40	LGATE2	Channel 2 LS driver output. A little series resistor helps in reducing device-dissipated power.
41	VCCDR2	Channel 2 LS driver supply: it can be varied from 5V to 12V buses. It must be connected together with other VCCDRx pins. Filter locally with at least 1µF ceramic cap vs. PGND2.
42	PHASE2	Channel 2 HS driver return path. It must be connected to the HS2 mosfet source and provides the return path for the HS driver of channel 2.
43	UGATE2	Channel 2 HS driver output. A little series resistor helps in reducing device-dissipated power.
44	BOOT2	Channel 2 HS driver supply. This pin supplies the relative high side driver. Connect through a capacitor (100nF Typ.) to the PHASE2 pin and through a diode to VCC (cathode vs. boot).

Table 1. Pins description (continued)

N°	Name	Description
45	BOOT1	Channel 1 HS driver supply. This pin supplies the relative high side driver. Connect through a capacitor (100nF Typ.) to the PHASE1 pin and through a diode to VCC (cathode vs. boot).
46	UGATE1	Channel 1 HS driver output. A little series resistor helps in reducing device-dissipated power.
47	PHASE1	Channel 1 HS driver return path. It must be connected to the HS1 mosfet source and provides the return path for the HS driver of channel 1.
48	N.C.	Not internally connected.
PAD	THERMAL PAD	Thermal pad connects the silicon substrate and makes a good thermal contact with the PCB to dissipate the power necessary to drive the external mosfets. Connect to the GND plane with several vias to improve thermal conductivity.

3 Maximum ratings

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}, VCCDRx	To PGNDx	15	V
V_{BOOTx}- V_{PHASEx}	Boot Voltage	15	V
V_{UGATEx}- V_{PHASEx}		15	V
	LGATEx, PHASEx to PGNDx	-0.3 to Vcc+0.3	V
	VID0 to VID5	-0.3 to 5	V
	All other pins to PGNDx	-0.3 to 7	V
V_{PHASEx}	Sustainable Positive Peak Voltage. T<20nS @ 600kHz	26	V
CS3- Pin	Maximum Withstanding Voltage Range Test Condition: CDF-AEC-Q100-002"Human Body Model" Acceptance Criteria: "Normal Performance"	±1500	V
OTHER PINS		±2000	V

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal Resistance Junction to Ambient (Device soldered on 2s2p PC Board)	40	°C / W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction Temperature Range	0 to 125	°C
P_{TOT}	Max power dissipation at T_A = 25°C	2.5	W

4 Electrical specifications

Table 4. Electrical characteristcs
(V_{CC}=12V±15%, T_J = 0°C to 70°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CC} supply current						
I_{CC}	VCC supply current	HGATEx and LGATEx open VCCDRx=VBOOTx=12V		18	23	mA
I_{CCDRx}	VCCDRx supply current	LGATEx open; VCCDRx=12V		1.5	2	mA
I_{BOOTx}	BOOTx supply current	HGATEx open;PHASEx to PGNDx VCC=BOOTx=12V		1	1.5	mA
Power-ON						
	Turn-On VCC threshold	VCC Rising; VCCDRx=5V	8.2	9.2	10.2	V
	Turn-Off VCC threshold	VCC Falling; VCCDRx=5V	6.5	7.5	8.5	V
	Turn-On VCCDRx Threshold	VCCDRx Rising VCC=12V	4.2	4.4	4.6	V
	Turn-Off VCCDRx Threshold	VCCDRx Falling VCC=12V	4.0	4.2	4.4	V
Oscillator and inhibit						
f_{OSC}	Initial Accuracy	OSC = OPEN OSC = OPEN; T_J=0 to 125°C	135 127	150	165 178	kHz kHz
$OUTEN_{IL}$	Output Enable Threshold	Input Low			0.3	V
$OUTEN_{IH}$		Input High	0.5			V
d_{MAX}	Maximum duty cycle	OSC = OPEN: CS_SEL = OPEN; I_{FB}=0	72	80		%
		OSC = OPEN; CS_SEL = OPEN; I_{FB}=105µA	30	40		%
ΔVosc	Ramp Amplitude			3		V
FAULT	Voltage at pin OSC	OVP or UVP Active	4.70	5.0	5.30	V

Table 4. Electrical characteristcs (continued)
(V_{CC}=12V±15%, T_J = 0°C to 70°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Reference and DAC						
	Output Voltage Accuracy	VRD10.x DAC FBR = VOUT; FBG = GNDOUT	-0.5	-	0.5	%
		HAMMER DAC FBR = VOUT; FBG = GNDOUT	-0.6	-	0.6	%
I_{VID}, I_{VID_SEL}	VID, VID_SEL pull-up Current	VIDx = GND VID_SEL=GND	3	4.5	6	µA
	VID, VID_SEL pull-up Voltage	VIDx = OPEN VID_SEL = OPEN		3		V
VID_{IL}	VID, VID_SEL Threshold	Input Low			0.4	V
VID_{IH}		Input High	0.8			V
Error amplifier						
A_0	DC Gain			80		dB
SR	Slew-Rate	COMP = 10pF		15		V/µs
Differential amplifier (remote buffer)						
	DC Gain			1		V/V
CMRR	Common Mode Rejection Ratio			40		dB
SR	Slew Rate	VSEN = 10pF		15		V/µs
Differential current sensing and offset						
I_{CSx-}	Bias Current	I_{LOAD} = 0		50		µA
I_{CSx+}	Bias Current			50		µA
$\frac{NFOx - I_{AVG}}{I_{AVG}}$	Current Sense Mismatch		-3	-	3	•%
I_{OCTH}	Over Current Threshold	I_{CSx-}(OCP)-I_{CSx-}(0)	30	35	40	µA
I_{FB}	Droop Current deviation from nominal value	OFFSET = TC = SGND I_{FB} = 0 to 75µA	-3.5	-	+3.5	µA
	Offset Current	I_{LOAD}=0; I_{OFFSET} =100µA; TC = SGND	-90	-100	-110	µA
		I_{LOAD}=0; I_{OFFSET} =100mA; TC Enabled	90	100	110	µA
I_{OFFSET}	OFFSET pin Current Range		0	-	250	µA
V_{OFFSET}	OFFSET pin Voltage	I_{OFFSET} = 0 to 250µA		1.240		V

Table 4. Electrical characteristcs (continued)
(V_{CC}=12V±15%, T_J = 0°C to 70°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Thermal sensor						
V_{TC}	TC Voltage at T_{amb} = 27ºC	R_{TC}=100kΩ R_{TC}=50kΩ R_{TC}=5kΩ	0.612 0.593 0.530	0.645 0.625 0.558	0.677 0.656 0.586	V
Gate drivers						
$t_{RISE\ HGATE}$	High Side Rise Time	BOOTx-PHASEx=10V; C_{HGATEx} to PHASEx=3.3nF		15	30	ns
I_{HGATEx}	High Side Source Current	BOOTx-PHASEx=10V		2		A
R_{HGATEx}	High Side Sink Resistance	BOOTx-PHASEx=12V;	1.5	2	2.5	Ω
$t_{RISE\ LGATE}$	Low Side Rise Time	VCCDRx=10V; C_{LGATEx} to PGNDx=5.6nF		30	55	ns
I_{LGATEx}	Low Side Source Current	VCCDRx=10V		1.8		A
R_{LGATEx}	Low Side Sink Resistance	VCCDRx=12V	0.7	1.1	1.5	Ω
Protections and SS_END						
V_{SS_ENDL}	SS_END Voltage Low	I_{SS_END} = -4mA			0.4	V
I_{SS_ENDH}	SS_END Leakage	V_{SS_END} = 5V			1	µA
UVP	Under Voltage Trip	VSEN Falling	55	60	65	%
OVP	Over Voltage Threshold	VSEN Rising; OVP = OPEN	112	115	118	%
	Over Voltage Threshold	VSEN Rising; OVP = 90kΩ• to SGND	1.54	1.64	1.74	V
Preliminary OVP	Turn-ON Threshold	VCC = VCCDRx Rising		4		V
	PreOVP Threshold	FBR Rising		1.8		V
	PreOVP Hysteresis			350		mV

5 VID Tables

Table 5. Voltage IDentification (VID) Codes.

VID_SEL = OPEN (VRD 10.x DAC with -19mV auto-offset)													
VID5	VID4	VID3	VID2	VID1	VID0	Output (V)	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	0	1	0	1	0	0.8185	0	1	1	0	1	0	1.1935
1	0	1	0	0	1	0.8310	1	1	1	0	0	1	1.2060
0	0	1	0	0	1	0.8435	0	1	1	0	0	1	1.2185
1	0	1	0	0	0	0.8560	1	1	1	0	0	0	1.2310
0	0	1	0	0	0	0.8685	0	1	1	0	0	0	1.2435
1	0	0	1	1	1	0.8810	1	1	0	1	1	1	1.2560
0	0	0	1	1	1	0.8935	0	1	0	1	1	1	1.2685
1	0	0	1	1	0	0.9060	1	1	0	1	1	0	1.2810
0	0	0	1	1	0	0.9185	0	1	0	1	1	0	1.2935
1	0	0	1	0	1	0.9310	1	1	0	1	0	1	1.3060
0	0	0	1	0	1	0.9435	0	1	0	1	0	1	1.3185
1	0	0	1	0	0	0.9560	1	1	0	1	0	0	1.3310
0	0	0	1	0	0	0.9685	0	1	0	1	0	0	1.3435
1	0	0	0	1	1	0.9810	1	1	0	0	1	1	1.3560
0	0	0	0	1	1	0.9935	0	1	0	0	1	1	1.3685
1	0	0	0	1	0	1.0060	1	1	0	0	1	0	1.3810
0	0	0	0	1	0	1.0185	0	1	0	0	1	0	1.3935
1	0	0	0	0	1	1.0310	1	1	0	0	0	1	1.4060
0	0	0	0	0	1	1.0435	0	1	0	0	0	1	1.4185
1	0	0	0	0	0	1.0560	1	1	0	0	0	0	1.4310
0	0	0	0	0	0	1.0685	0	1	0	0	0	0	1.4435
1	1	1	1	1	1	OFF	1	0	1	1	1	1	1.4560
0	1	1	1	1	1	OFF	0	0	1	1	1	1	1.4685
1	1	1	1	1	0	1.0810	1	0	1	1	1	0	1.4810
0	1	1	1	1	0	1.0935	0	0	1	1	1	0	1.4935
1	1	1	1	0	1	1.1060	1	0	1	1	0	1	1.5060
0	1	1	1	0	1	1.1185	0	0	1	1	0	1	1.5185
1	1	1	1	0	0	1.1310	1	0	1	1	0	0	1.5310
0	1	1	1	0	0	1.1435	0	0	1	1	0	0	1.5435
1	1	1	0	1	1	1.1560	1	0	1	0	1	1	1.5560
0	1	1	0	1	1	1.1685	0	0	1	0	1	1	1.5685
1	1	1	0	1	0	1.1810	1	0	1	0	1	0	1.5810

Note: Since the VIDx pins program the maximum output voltage, according to VRD 10.x specs, the device automatically regulates to a voltage 19mV lower avoiding use of any external component to lower the regulated voltage. This improves the system tolerance performance since the reference already offset is trimmed during production within ±0.5%.

Table 6. Voltage IDentification (VID) Codes.

VID_SEL = SGND (Hammer DAC)													
HAMMER DAC							HAMMER DAC +25mV						
VID5	VID4	VID3	VID2	VID1	VID0	Output (V)	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
1	0	0	0	0	0	1.550	0	0	0	0	0	0	1.575
	0	0	0	0	1	1.525		0	0	0	0	1	1.550
	0	0	0	1	0	1.500		0	0	0	1	0	1.525
	0	0	0	1	1	1.475		0	0	0	1	1	1.500
	0	0	1	0	0	1.450		0	0	1	0	0	1.475
	0	0	1	0	1	1.425		0	0	1	0	1	1.450
	0	0	1	1	0	1.400		0	0	1	1	0	1.425
	0	0	1	1	1	1.375		0	0	1	1	1	1.400
	0	1	0	0	0	1.350		0	1	0	0	0	1.375
	0	1	0	0	1	1.325		0	1	0	0	1	1.350
	0	1	0	1	0	1.300		0	1	0	1	0	1.325
	0	1	0	1	1	1.275		0	1	0	1	1	1.300
	0	1	1	0	0	1.250		0	1	1	0	0	1.275
	0	1	1	0	1	1.225		0	1	1	0	1	1.250
	0	1	1	1	0	1.200		0	1	1	1	0	1.225
	0	1	1	1	1	1.175		0	1	1	1	1	1.200
	1	0	0	0	0	1.150		1	0	0	0	0	1.175
	1	0	0	0	1	1.125		1	0	0	0	1	1.150
	1	0	0	1	0	1.100		1	0	0	1	0	1.125
	1	0	0	1	1	1.075		1	0	0	1	1	1.100
	1	0	1	0	0	1.050		1	0	1	0	0	1.075
	1	0	1	0	1	1.025		1	0	1	0	1	1.050
	1	0	1	1	0	1.000		1	0	1	1	0	1.025
	1	0	1	1	1	0.975		1	0	1	1	1	1.000
	1	1	0	0	0	0.950		1	1	0	0	0	0.975
	1	1	0	0	1	0.925		1	1	0	0	1	0.950
	1	1	0	1	0	0.900		1	1	0	1	0	0.925
	1	1	0	1	1	0.875		1	1	0	1	1	0.900
	1	1	1	0	0	0.850		1	1	1	0	0	0.875
	1	1	1	0	1	0.825		1	1	1	0	1	0.850
	1	1	1	1	0	0.800		1	1	1	1	0	0.825
	1	1	1	1	1	OFF		1	1	1	1	1	OFF

6 Device description

The device is a three phase PWM controller with embedded high current drivers that provides complete control logic and protections for a high performance step-down DC-DC voltage regulator optimized for advanced microprocessor power supply. Multi phase buck is the simplest and most cost-effective topology employable to satisfy the increasing current demand of newer microprocessors and modern high current DC/DC converters and POLs. It allows distributing equally load and power between the phases using smaller, cheaper and most common external power mosfets and inductors. Moreover, thanks to the 120° of phase shift between each phase, the input and output capacitor count results in being reduced. Phase interleaving causes in fact input rms current and output ripple voltage reduction and show an effective output switching frequency increase: the 150kHz free-running frequency per phase, externally adjustable through a resistor, results tripled on the output.

The controller includes multiple DACs, selectable through an apposite pin (VID_SEL), allowing compatibility with both VRD 10.x and Hammer specifications, also performing D-VID transitions accordingly. The output voltage can be precisely selected, programming the VID and VID_SEL pins, from 0.8185V to 1.5810V with 12.5mV binary steps (VRD 10.x compliant mode - 6 BIT with -19mV offset already programmed during production) or from 0.800V to 1.550V with 25mV steps (VRM Hammer compliant mode - 5 BIT, VID5 programs a 25mV positive offset in this case), with a maximum tolerance on the output regulated voltage of ±0.5% (±0.6% for Hammer) over temperature and line voltage variations.

The device permits easy and flexible system design by allowing current reading across either inductor or low side mosfet in fully differential mode simply selecting the desired way through the CS_SEL pin. In both cases, also a sense resistor in series to the related element can be considered to improve reading precision. The current information read corrects the PWM output in order to equalize the average current carried by each phase limiting the error at ±3% over static and dynamic conditions unless considering the sensing element spread.

The device provides a programmable Over-Voltage protection to protect the load from dangerous over stress and can be externally set to a fixed voltage through an apposite resistor or it can be set internally with a fixed percentage, latching immediately by turning ON the lower driver and driving high the FAULT pin. Furthermore, preliminary OVP protection also allows the device to protect load from dangerous OVP when VCC is not above the UVLO threshold.

Over-Current protection provided, with an OC threshold for each phase, causes the device to enter in constant current mode until the latched UVP. Depending on the reading mode selected, the device keeps constant the peak (inductor sensing) or the valley (LS sensing) of the inductor current ripple.

The device drives high the FAULT pin after each latching event: to recover it is enough to cycle VCC or the OUTEN pin.

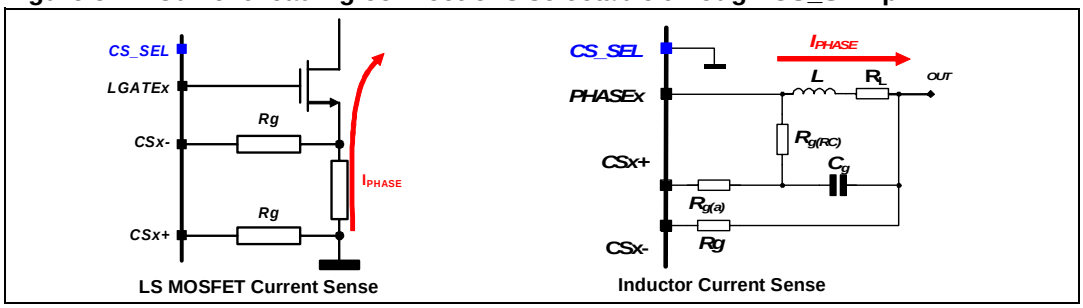
A compact 7x7mm body TQFP48 package with exposed thermal pad allows dissipating the power to drive the external mosfet through the system board.

7 Current reading and current sharing control loop

The device embeds a flexible, fully-differential current sense circuitry that is able to read across both low side or inductor parasitic resistance or across a sense resistor placed in series to that element. The fully-differential current reading rejects noise and allows placing sensing element in different locations without affecting the measurement's accuracy. The kind of sense element can be simply chosen through the CS_SEL pin: setting this pin free, the LS mosfet is used while shorting it to SGND, the inductor will be used instead. Details about connections are shown in *Figure 5*.

The high bandwidth current sharing control loop allows current balance even during load transients: a current reference equal to the average of the read current (I_{AVG}) is internally built and the error between the read current and this reference is converted to a voltage that with a proper gain is used to adjust the duty cycle whose dominant value is set by the voltage error amplifier.

Figure 5. Current reading connections selectable through CS_SEL pin.



7.1 Low-side current reading

Leaving CS_SEL pin OPEN, the current flowing trough each phase is read using the voltage drop across the low side mosfets R_{dsON} or across a sense resistor in its series and it is internally converted into a current. The transconductance ratio is issued by the external resistor Rg placed outside the chip between CSx- and CSx+ pins toward the reading points (see *Figure 6* right). The proprietary current sense circuit tracks the current information for a time $T_{TRACK} = T_{SW}/3$ ($T_{SW} = 1/F_{SW}$) centered in the middle of the low-side mosfet conduction time (OFF Time, see *Figure 6 left*) and holds the tracked information during the rest of the period.

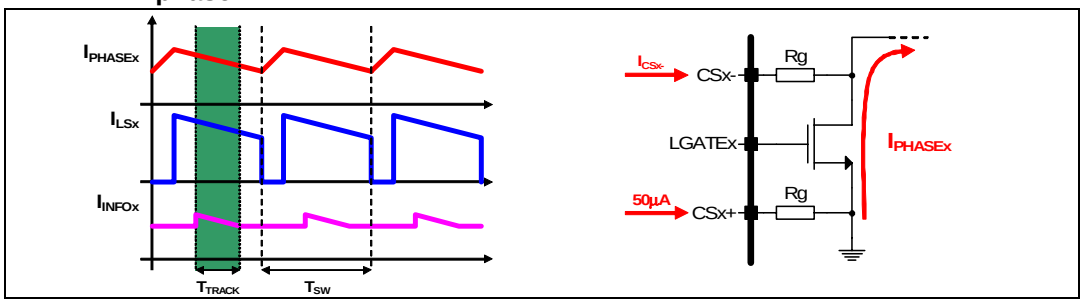
This device sources a constant 50µA current from the CSx+ pin: the current reading circuitry uses this pin as a reference and the reaction keeps the CSx- pin to this voltage during the reading time (an internal clamp keeps CSx+ and CSx- at the same voltage sinking from the CSx- pin the necessary current during the hold time; this is needed when LS mosfet R_{dsON} sense is implemented to avoid absolute maximum rating overcome on CSx- pin). The current that flows from the CSx- pin is then given by the following equation (See *Figure 6 - right*):

$$I_{CSx-} = 50\mu A + \frac{R_{dsON}}{R_g} \cdot I_{PHASEx} = 50\mu A + I_{INFOx} \quad \text{where: } I_{INFOx} = \frac{R_{dsON}}{R_g} \cdot I_{PHASEx}$$

R_{dsON} is the on resistance of the low side mosfet and Rg is the transconductance resistor used between CSx- and CSx+ pins toward the reading points; I_{PHASEx} is the current carried by the relative phase and I_{INFOx} is the current information signal reproduced internally.

50µA offset allows negative current reading, enabling the device to check for dangerous returning current between the phases assuring the complete current equalization. From the current information of each phase, information about the total current delivered (I_{DROOP} = I_{INFO1} + I_{INFO2} + I_{INFO3}) and the average current for each phase (I_{AVG} = (I_{INFO1} + I_{INFO2} + I_{INFO3})/3) is taken. I_{INFOX} is then compared to I_{AVG} to give the correction to the PWMx output in order to equalize the current carried by the three phases.

Figure 6. Current reading across LS mosfet: timing (left) and circuit (right) for each phase.



7.2 Inductor current reading

Shorting CS_SEL pin to SGND, the current flowing trough each phase is read using the voltage drop across the output inductor or across a sense resistor (R_{SENSE}) in its series and internally converted into a current. The transconductance ratio is issued by the external resistor Rg placed outside the chip between CSx- and CSx+ pins toward the reading points (see *Figure 5* right).

The current sense circuit always tracks the current sensed and still sources a constant 50µA current from the CSx+ pin: this pin is used as a reference keeping the CSx- pin to this voltage. To correctly reproduce the inductor current an R-C filtering network must be introduced in parallel to the sensing element.

The current that flows from the CSx- pin is then given by the following equation (See *Figure 7*):

$$I_{CSx-} = 50\mu A + \frac{R_L}{R_g} \cdot \left(\frac{1 + s \cdot \frac{L}{R_L}}{1 + s \cdot R_{g(RC)} \cdot Cg} \right) \cdot I_{PHASEx}$$

Where IP_{HASEx} is the current carried by the relative phase.

Considering now to match the time constant between the inductor and the R-C filter applied (Time constant mismatches cause the introduction of poles into the current reading network causing instability. Moreover, it is also important for the load transient response and to let the system show resistive equivalent output impedance), it results:

$$R_{g(RC)} \cdot Cg \geq I_{CSx-} = 50\mu A + \frac{R_L}{Rg} \cdot I_{PHASEx} = 50\mu A + I_{INFOx} \text{ where } I_{INFOx} = I_{PHASEx} \cdot \frac{R_L}{Rg}$$

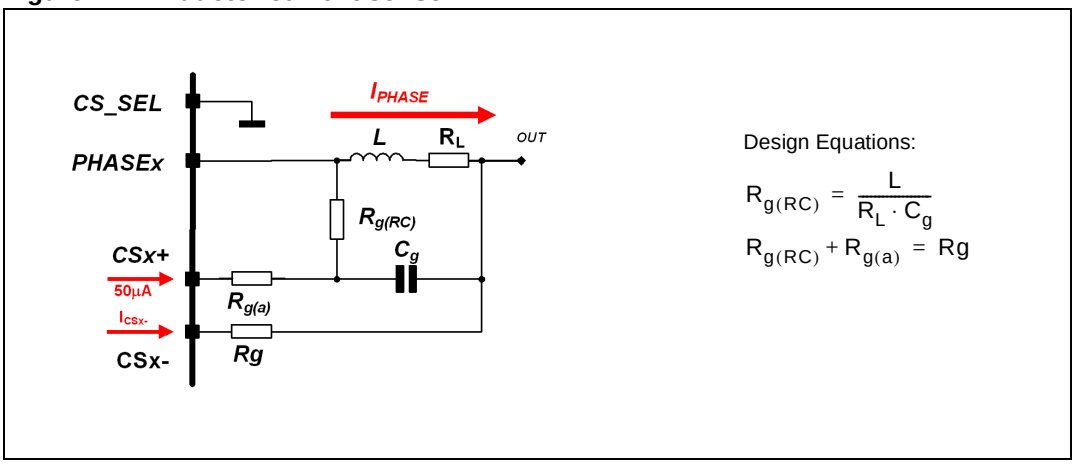
I_{INFOx} is the current information reproduced internally.

50µA offset allows negative current reading, enabling the device to check for dangerous returning current between the phases assuring the complete current equalization. From the

current information of each phase, information about the total current delivered (I_{DROOP} = I_{INFO1} +I_{INFO2} + I_{INFO3}) and the average current for each phase (I_{AVG} = (I_{INFO1} + I_{INFO2} + I_{INFO3})/3) is taken. I_{INFOX} is then compared to I_{AVG} to give the correction to the PWM output in order to equalize the current carried by the three phases.

Since Rg is designed considering the OC protection, to allow further flexibility in the system design, the resistor in series to CSx+ can be split in two resistors as shown in *Figure 7*.

Figure 7. Inductor current sense



8 DAC Selection

The device embeds a selectable DAC that allows the output voltage to have a tolerance of ±0.5% (0.6% for Hammer DAC) recovering from offsets and manufacturing variations. The VID_SEL pin selects the DAC table used to program the reference for the regulation as shown in *Table* .

Table 7. DAC Selection

VID_SEL	Selected DAC	
OPEN	VRM / VRD 10.x DAC. Output voltage ranges from 0.8185V to 1.5810V with 12.5mV steps (See *Table 5*). Since the VIDx pins program the maximum output voltage, according to VRD 10.x specs, the device automatically regulates with –19mV offset avoiding use of any external component to lower the regulated voltage. Since the -19mV offset is programmed during the production stage, no further error is introduced to generate the offset since it is automatically recovered during the trimming stage.	
SGND	**VID5**	**Hammer DAC**
	OPEN	Output voltage ranges from 0.800V to 1.550V with 25mV steps (See *Table 6*).
	SGND	Output voltage ranges from 0.825V to 1.575V with 25mV steps (See *Table 6*). Since the +25mV offset is programmed during the production stage, no further error is introduced to generate the offset since it is automatically recovered during the trimming stage.

VID pins are inputs of an internal DAC that is realized by means of a series of resistors providing a partition of the internal voltage reference. The VID code drives a multiplexer that selects a voltage on a precise point of the divider. The DAC output is delivered to an amplifier obtaining the voltage reference (i.e. the set-point of the error amplifier, V_{PROG}). Internal pull-ups are provided (realized with a 5µA current generator up to 3V Typ); in this way, to program a logic "1" it is enough to leave the pin floating, while to program a logic "0" it is enough to short the pin to SGND.

Programming the "11111x" code (NOCPU, VID5 is irrelevant), the device shuts down: all mosfets are turned OFF and SS_END is shorted to SGND. Removing the code causes the device to restart.

The voltage identification (VID) pin configuration also sets the Over / Under Voltage protection (OVP/UVP) thresholds.

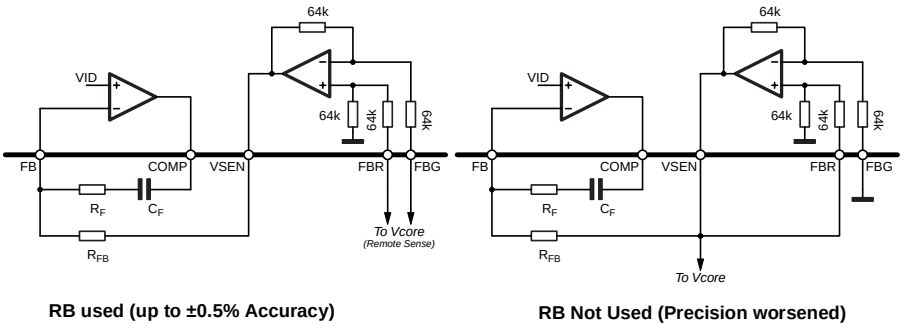
9 Remote voltage sense

The device embeds a Remote Sense Buffer to sense remotely the regulated voltage without any additional external components. In this way, the output voltage programmed is regulated between the remote buffer inputs compensating motherboard or connector losses. The very low-offset amplifier senses the output voltage remotely through the pins FBR and FBG (FBR is for the regulated voltage sense while FBG is for the ground sense) and reports this voltage internally at VSEN pin with unity gain eliminating the errors. Keeping the FBR and FBG traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

If remote sense is not required, it is enough connecting the resistor R_{FB} directly to the regulated voltage: VSEN becomes not connected and still senses the output voltage through the remote buffer. In this case the FBG and FBR pins must be connected anyway to the regulated voltage (See *Figure 8*).

Warning: The remote buffer is included in the trimming chain in order to achieve ±0.5% accuracy (0.6% for the Hammer DAC) on the output voltage when the RB is used: eliminating it from the control loop causes the regulation error to be increased by the RB offset worsening the device performances!

Figure 8. Remote buffer connections



10 Voltage positioning

Output voltage positioning is performed by selecting the reference DAC and by programming the different contributors to the I_{FB} current (see *Figure 9*). This current, sourced from the FB pin, causes the output voltage to vary according to the external R_{FB} resistor: this allows programming precise output voltage variations depending on the sensed current (Droop Function) as well as offsets for the regulation.

The three contributors to the I_{FB} current value are:

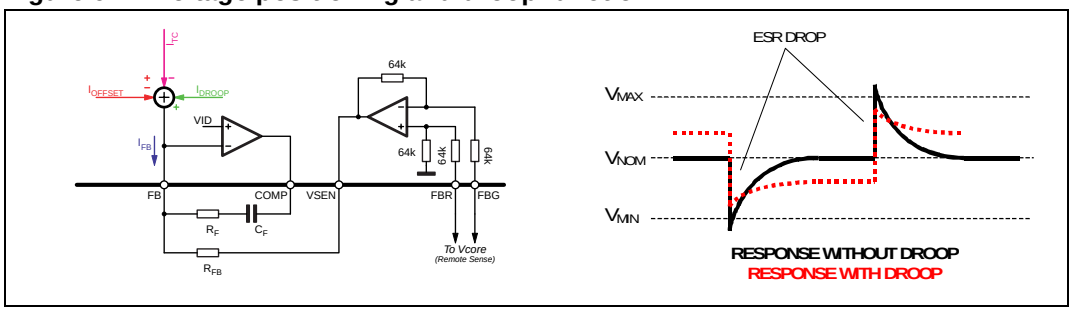
- Droop Function (green);
- Offset (red);
- Integrated Temperature Compensation (fuchsia).

Moreover, the embedded Remote Buffer allows to precisely programming the output voltage offsets and variations by recovering the voltage drops across distribution lines.

The output voltage is then driven by the following relationship (I_{OFFSET} sign depends on TC setting):

$$VID - R_{FB} \cdot I_{FB} = VID - R_{FB} \cdot (I_{DROOP} \pm I_{OFFSET} - I_{TC})$$

Figure 9. Voltage positioning and droop function



10.1 Droop function

Droop function allows the device to satisfy the requirements of high performance microprocessors, reducing the size and the cost of the output capacitor. This method "recovers" part of the drop due to the output capacitor ESR in the load transient, introducing a dependence of the output voltage on the load current: a static error proportional to the output current causes the output voltage to vary according to the sensed current. As shown in figure 4-right, the ESR drop is present in any case, but using the droop function the total deviation of the output voltage is minimized.

The information about the total current delivered (I_{DROOP}) is sourced from the FB pin (see *Figure 9*): connecting a resistor between this pin and VSEN (i.e. the output voltage), the total current information flows only in this resistor because the compensation network between FB and COMP has always a capacitor in series (C_F, see *Figure 9*). The voltage regulated is then equal to:

$$V_{OUT} = VID - R_{FB} \cdot I_{DROOP}$$

Where VID is the reference programmed through VIDx and VID_SEL (Only the I_{DROOP} contribute to I_{FB} has been considered).

Since I_{DROOP} depends on the current information about the three phases, the output characteristic vs. load current is given by:

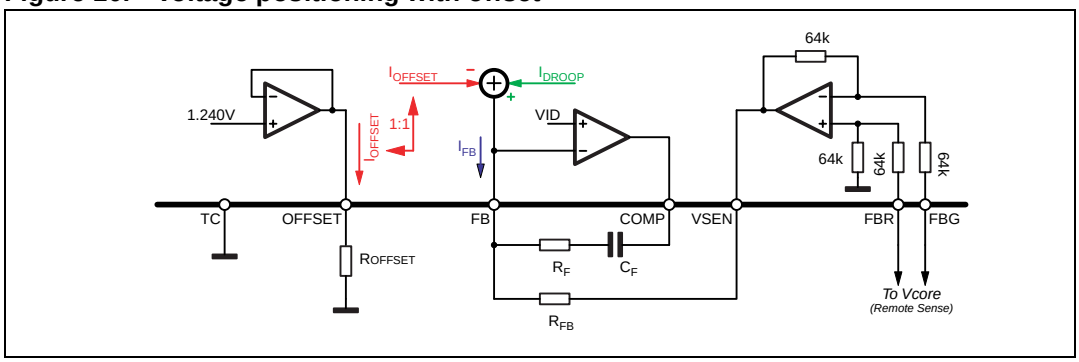
$$VID - R_{FB} \cdot I_{DROOP} = VID - R_{FB} \cdot \frac{R_{SENSE}}{Rg} \cdot I_{OUT} = VID - R_{DROOP} \cdot I_{OUT}$$

Where R_{SENSE} is the chosen sensing element resistance (Inductor DCR or LS R_{dsON}), I_{OUT} is the output current of the system and R_{DROOP} is its equivalent output resistance (The whole power supply can be then represented by a "real" voltage generator with a voltage value of VID and an equivalent series resistance R_{DROOP}).

R_{FB} resistor can be also designed according to the R_{DROOP} specifications as follow:

$$R_{FB} = R_{DROOP} \cdot \frac{Rg}{R_{SENSE}}$$

Figure 10. Voltage positioning with offset



10.2 Offset

The OFFSET pin allows programming a positive or a negative offset (V_{OS}) for the output voltage.

When the Integrated Thermal Sensor is disabled (TC = SGND) a resistor R_{OFFSET} connected vs. SGND increases the output voltage: since the pin is internally fixed at 1.240V, the current programmed by the resistor R_{OFFSET} is mirrored and then properly subtracted from the I_{FB} current (see *Figure 10*) as follow (Only the I_{OFFSET} contribute to I_{FB} has been considered):

$$V_{OUT} = VID + R_{FB} \cdot I_{OFFSET} = VID + R_{FB} \cdot \left(\frac{1.240V}{R_{OFFSET}}\right) = VID + V_{OS}$$

The device will add the programmed offset V_{OS} to the output programmed voltage (considering now also the droop effect) subtracting the relative offset current from the feedback current I_{FB}:

$$VID - R_{FB} \cdot I_{FB} = VID - R_{FB} \cdot (I_{DROOP} - I_{OFFSET}) = VID + R_{FB} \cdot I_{OFFSET} - R_{DROOP} \cdot I_{OUT}$$

Offset resistor can be designed by considering the following relationship (R_{FB} is fixed by the Droop effect):

$$R_{OFFSET} = \frac{1.240V}{V_{OS}} \cdot R_{FB}$$

Offset automatically given by the DAC selection or by VID5 when VID_SEL=SGND differs from the offset implemented through the OFFSET pin: the built-in feature is trimmed in production and assures ±0.5% error (±0.6% for the Hammer DAC) over load and line variations while implementing the same offset through the OFFSET pin causes additional errors to be considered in the total output voltage precision.

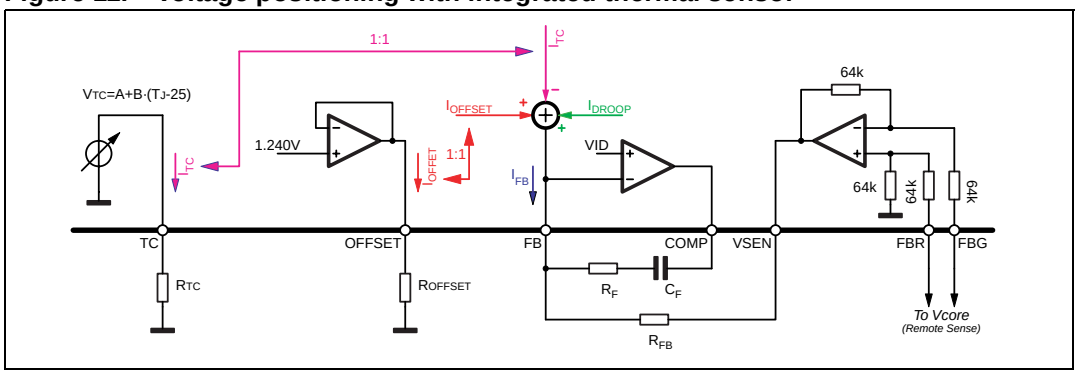
When the Integrated Thermal Sensor is enabled (see *Figure 11* and following section), the pin programs, in the same way as before, a negative offset. This is to compensate the positive native offset introduced by the ITS. The effect of the programmed offset on the output voltage results (I_{OFFSET} is now added to I_{FB} and no more subtracted as before):

$$V_{OUT} = VID - R_{FB} \cdot I_{OFFSET} = VID - R_{FB} \cdot \left(\frac{1.240}{R_{OFFSET}}\right) = VID - V_{OS}$$

Offset resistor is designed to compensate the ITS native offset as described in the following section.

The Offset function can be disabled by shorting the pin to SGND.

Figure 11. Voltage positioning with integrated thermal sensor



10.3 Integrated thermal sensor

Current sense elements have non-negligible temperature variations: considering either inductor or LS mosfet sense, the sensing elements modify proportionally to varying temperature. As a consequence, the sensed current is subjected to a measurement error that causes the regulated voltage to vary accordingly.

To recover from this temperature related error, a temperature compensation circuit is integrated into the controller: the internal temperature is sensed and the droop current is corrected (according to a scaling external resistor R_{TC}) in order to keep constant the regulated voltage.

The ITS circuit subtracts from the I_{FB} current a current proportional to the sensed temperature as follow (see *Figure 11*, Only the I_{DROOP} and I_{TC} contributes to I_{FB} have been considered):

$$V_{OUT}(T,I_{OUT}) = VID - R_{FB} \cdot \left[\frac{R_{SENSE}(T_{MOS})}{Rg} \cdot I_{OUT} - I_{TC}(T_J)\right]$$

where $I_{TC}(T_J) = \frac{1}{R_{TC}} \cdot [A + B \cdot (T_J - 25)]$

where A and B are positive constants depending on the value of the external resistor R_{TC} (see *Figure 12*), T_J is the device junction temperature and T_{MOS} is the mosfet (or the used sensing element) temperature.

The resistor R_{TC} can be designed in order to zero the temperature influence on the output voltage at a fixed current as follow:

$$-R_{FB} \cdot \frac{R_{SENSE} \cdot \alpha \cdot (T_{MOS} - 25)}{Rg} \cdot I_{OUT} + \frac{R_{FB}}{R_{TC}} \cdot B \cdot (T_J - 25) = 0$$

obtaining the following relationship: $R_{TC} = \frac{Rg}{R_{SENSE}} \cdot \frac{B \cdot k_T}{\alpha \cdot I_{OUT}}$

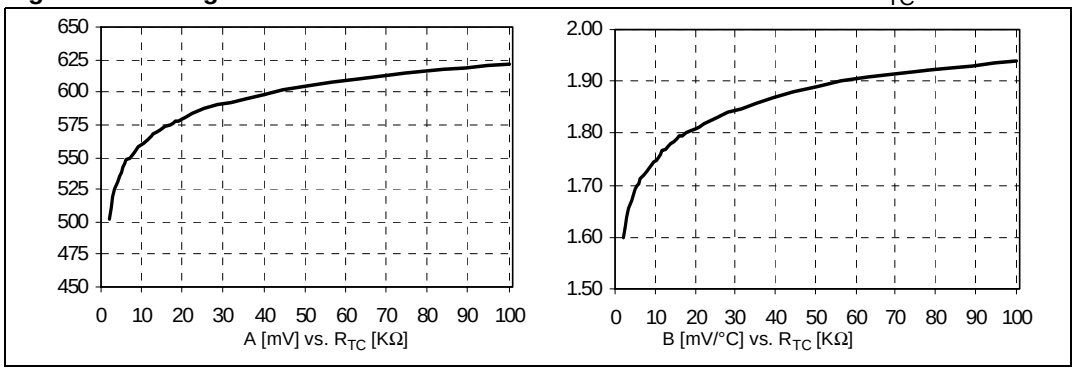
where R_{SENSE} is the sensing element resistance value (at T_{MOS} = 25ºC), B is the constant obtainable from

Figure 12, k_T is the Temperature Coupling Coefficient between the sensing element and the Controller (it results $K_T = (T_J\text{-}25)/(T_{MOS}\text{-}25)$) and α is the Temperature Coefficient of the sensing element. Since R_{TC} depends from the constant B depending in turn from R_{TC}, an iterative process is required to properly design the R_{TC} value. As a consequence of the nature of the thermal sensor, a negative offset is needed to compensate the native offset introduced by the ITS at a referenced temperature Tref and it is obtainable by connecting a R_{OFFSET} resistor between the OFFSET pin and SGND as follow:

$$I_{OFFSET} = -I_{TC}(T_{ref}) = \frac{A + B \cdot (T_{ref} - 25)}{R_{TC}}$$

To disable this function, short the pin to SGND.

Figure 12. Integrated thermal sensor constant vs. external resistor R_{TC}



11 Dynamic VID transitions

The device is able to manage Dynamic VID Code changes that allow Output Voltage modification during normal device operation.

OVP and UVP signals are masked during every VID transition and they are re-activated after the transition finishes.

When changing dynamically the regulated voltage (D-VID), the system needs to charge or discharge the output capacitor accordingly. This means that an extra-current $I_{D\text{-}VID}$ needs to be delivered, especially when increasing the output regulated voltage and it must be considered when setting the over current threshold. This current result:

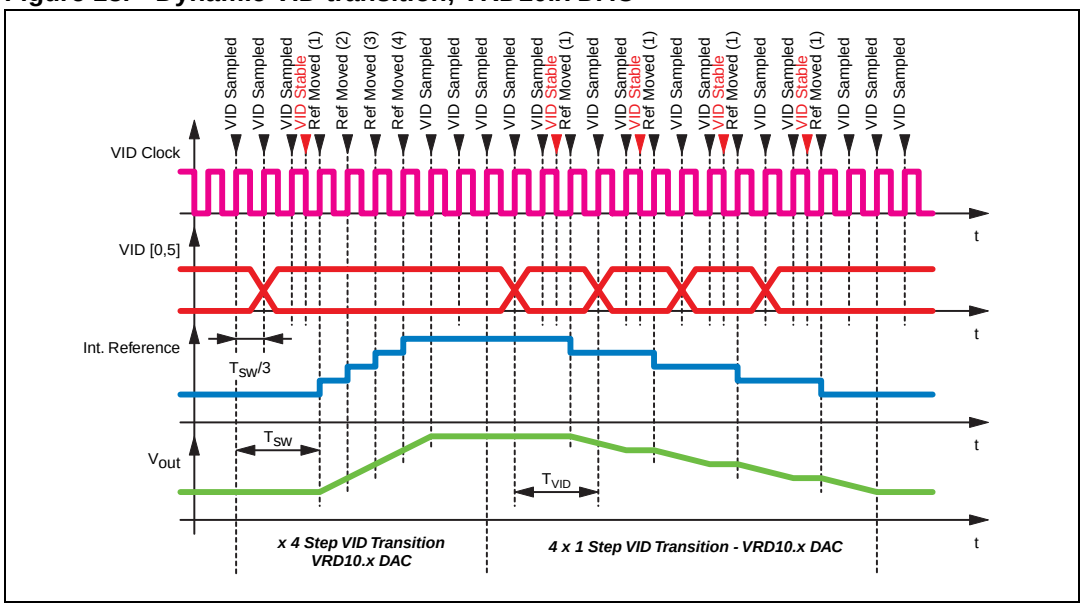
$$I_{D-VID} = \frac{C_{OUT} \cdot dV_{OUT}}{dT_{VID}}$$

where dV_{OUT} is the selected DAC LSB (12.5mV for VRD10.x or 25mV for Hammer DAC) and T_{VID} is the time interval between each LSB transition.

Overcoming the OC threshold during the dynamic VID causes the device to enter the constant current limitation slowing down the output voltage dV/dt also causing the failure in the D-VID test.

The way in which the device modifies the reference depends on the VID_SEL status and then on the kind of DAC selected.

Figure 13. Dynamic VID transition, VRD10.x DAC



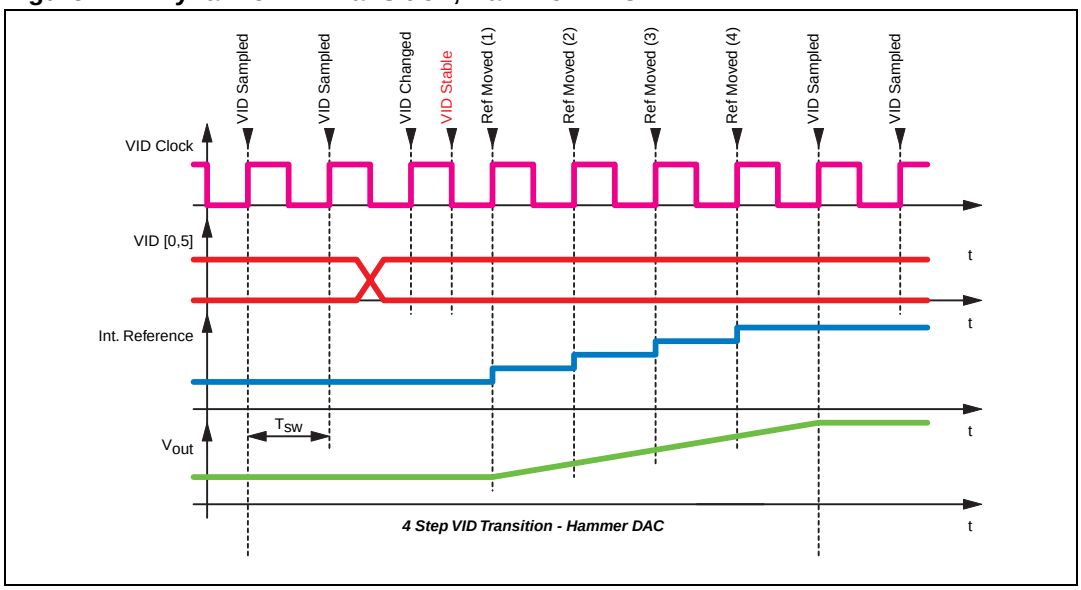
11.1 VID_SEL = OPEN.

Selecting the VRD10.x DAC, the device checks for VID code modifications on the rising edge of a clock that is three times the switching frequency of each phase and waits for a confirmation on the following falling edge. Once the new code is stable, on the next rising edge, the reference starts stepping up or down in LSB increments (12.5mV) every clock cycle (still $3 \cdot F_{SW}$) until the new VID code is reached. During the transition, VID code changes are ignored; the device re-starts monitoring VID after the transition has finished on the next rising edge available.

Warning: **if the new VID code is more than 1 LSB higher than the previous, the device will execute the transition stepping the reference with a frequency equal to $3 \cdot F_{SW}$ until the new code has reached: for this reason it is recommended to carefully control the VID change rate in order to carefully control the slope of the output voltage variation.**

Warning: **DVID sample and hold clock depends on the switching frequency F_{SW}. To correctly perform DVID transition so following the VID change rate, it is required to have at least 2 complete cycles of the F_{DVID} clock between every VID transition. If the VID update-rate is, for example, 5µs, the minimum operating frequency results to be F_{SW} > 133kHz.**

Figure 14. Dynamic VID Transition, Hammer DAC



11.2 VID_SEL = GND.

Selecting the HAMMER DAC, the device checks for VID code modifications on the rising edge of a clock that is the same frequency of each phase and waits for a confirmation on the following falling edge. Once the new code is stable, on the next rising edge the reference starts stepping up or down in LSB increments (25mV) every clock cycle until the new VID code is reached. During the transition, VID code changes are ignored; the device re-starts monitoring VID after the transition has finished on the next rising edge.

If the new VID code is more than 1 bit higher than the previous, the device will execute the transition stepping the reference every switching cycle until the new code has reached

12 Enable and disable

The device has three different supplies: VCC pin to supply the internal control logic, VCCDRx to supply the low side drivers and BOOTx to supply the high side drivers. If the voltage at pins VCC and VCCDRx are not above the turn on thresholds specified in the Electrical Characteristics, the device is shut down: all drivers keep the mosfets off to show high impedance to the load. Once the device is correctly supplied, proper operation is assured but the device can be controlled in different ways:

- OUTEN pin. It can be used to control the power sequencing in complex systems. Setting the pin free, the device implements a soft start up to the programmed voltage. Shorting the pin to SGND, it resets the device (SS_END is shorted to SGND in this condition and protections are disabled except pre-OVP) from any latched condition and also disables the device keeping all the mosfet turned off to show high impedance to the load. It can be then cycled to recover from any latched condition such as OVP and UVP.
- NOCPU (VID [0;5]=11111x) In this condition (VID5 state is irrelevant) the device is disabled and keeps all the mosfet turned off to show high impedance to the load. Nevertheless, it waits for any VID code transition to power up implementing a soft start. During this condition, SS_END pin is shorted to SGND.

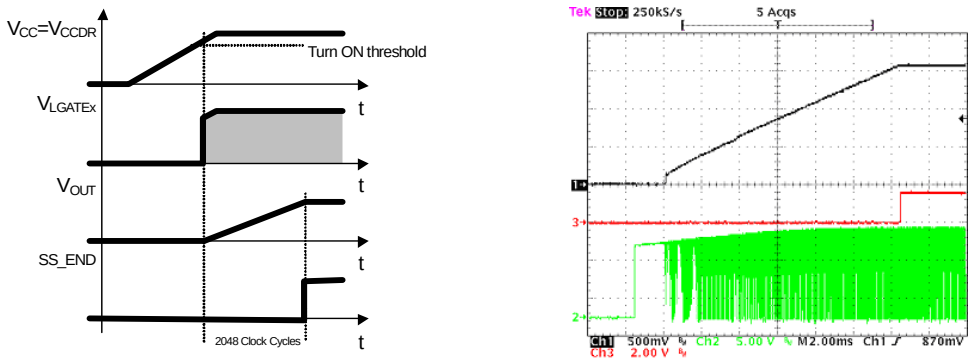
13 Soft start

During soft start, a ramp is generated increasing the loop reference from 0V to the final value programmed by VID in 2048 clock periods as shown in

Figure 15. Once the soft start begins, the reference is increased: upper and lower MOS begin to switch and the output voltage starts to increase with closed loop regulation. At the end of the digital soft start, the SS_END signal is then driven high.

The Under Voltage comparator is enabled when the reference voltage reaches 0.6V while Over Voltage Comparator is always enabled during soft start with a threshold equal to the 115% of the programmed reference or the threshold programmed by R_{OVP} (see relevant section).

Figure 15. Soft start



(CH1=VOUT; CH2=LGATEx; CH3=SS_END)

14 Output voltage monitor and protections

The device monitors through pin VSEN the regulated voltage in order to manage the OVP / UVP conditions.

14.1 UVP protection

If the output voltage monitored by VSEN drops below the 60% of the reference voltage for more than one clock period, the device turns off all mosfets and the OSC/FAULT is driven high (5V). The condition is latched; to recover it is required to cycle Vcc or the OUTEN pin.

14.2 Programmable OVP protection

Once VCC crosses the turn-ON threshold and the device is enabled (OUTEN = 1), the device provides a programmable Over Voltage protection; when the voltage sensed overcomes the programmed threshold, the controller permanently switches on all the low-side mosfets and switches off all the high-side mosfets in order to protect the load. The OSC/ FAULT pin is driven high (5V) and power supply or OUTEN pin cycling is required to restart operations.

The OVP threshold is programmed through the OVP pin: leaving the pin floating, it is internally pulled-up and the threshold is set at 115% (Typ.) of the programmed output voltage. Connecting the OVP pin to SGND through a resistor R_{OVP}, the OVP threshold becomes a fixed voltage as follow:

$O_{VPTH} = 1.455 \cdot R_{OVP} \cdot 12.5\mu$

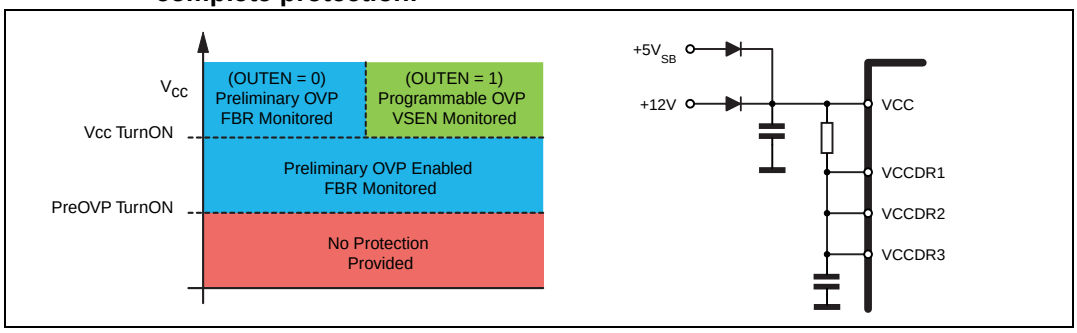
14.3 Preliminary OVP protection (Pre-OVP)

While VCC pin is under the turn-ON threshold, a preliminary-OVP protection turns on the low side mosfets as long as the FBR pin voltage is greater than 1.8V. This protection is enabled when VCC stays within the device turn-on threshold and the PreOVP turn on threshold and depends also on the OUTEN pin status as detailed in *Figure 16 - left*.

A simple way to provide protection to the output in all conditions when the device is OFF (then avoiding the unprotected red region in *Figure 16*) consists in supplying the controller through the $5V_{SB}$ bus as shown in *Figure 16 - right.*

Both Over Voltage and Under Voltage are active also during soft start (see the relevant section).

Figure 16. Output voltage protections and typical principle connections to assure complete protection.



14.4 Over current

Depending on the current reading method selected, the device limits the peak or the bottom of the inductor current entering in constant current until setting UVP as below explained.

The Over Current threshold has to be programmed, by designing the Rg resistors, to a safe value, in order to be sure that the device doesn't enter OCP during normal operation of the device. This value must take into consideration also the extra current needed during the Dynamic VID Transition $I_{D\text{-}VID}$ and, since the device reads across mosfets R_{dsON} or inductor DCR, the process spread and temperature variations of these sensing elements.

Moreover, since also the internal threshold spreads, the Rg design must consider its minimum value $I_{OCTH(min)}$ as follow:

$$Rg = \frac{I_{OCPx(max)} \cdot R_{SENSE(max)}}{I_{OCTH(min)}}$$

where $I_{OCP}x$ is the current measured by the current reading circuitry when the device enters Quasi Constant Current (LS Mosfet Sense) or Constant Current (Inductor Sense), I_{OCPx} must be calculated starting from the corresponding output current value $I_{OUT(OCP)}$ as follow ($I_{D\text{-}VID}$ must also be considered when D-VID are implemented):

$$I_{OCPx} = \begin{cases} \frac{I_{OUT(OCP)}}{3} - \frac{\Delta I_{pp}}{2} + \frac{I_{D\text{-}VID}}{3} & \text{Low Side Mosfet Sense} \\ \frac{I_{OUT(OCP)}}{3} + \frac{\Delta I_{pp}}{2} + \frac{I_{D\text{-}VID}}{3} & \text{Inductor DCR Sense} \end{cases}$$

where $I_{OUT(OCP)}$ is still the output current value at which the device enters Quasi Constant Current (LS Mosfet Sense) or Constant Current (Inductor Sense),ΔI_{PP} is the inductor current ripple in each phase and $I_{D\text{-}VID}$ is the additional current required by D-VID (when applicable). In particular, since the device limits the peak or the valley of the inductor current (according to CS_SEL status), the ripple entity, when not negligible, impacts on the real OC threshold value and must be considered.

14.5 Low side sense overcurrent (CS_SEL=OPEN)

The device detects an Over Current condition for each phase when the current information I_{INFOx} overcomes the fixed threshold of I_{OCTH} (35µA Typ). When this happens, the device keeps the relative LS mosfet on, skipping clock cycles, until the threshold is crossed back and IINFOx results being lower than the I_{OCTH} threshold. This implies that the device limits the bottom of each inductor current ripple.

After exiting the OC condition, the LS mosfet is turned off and the HS is turned on with a duty cycle driven by the PWM comparator.

Keeping the LS on, skipping clock cycles, causes the on-time subsequent to the exit from the OC condition to increase. Considering now that the device, with this kind of current sense, has maximum on-time dependence with the delivered current given by the following relationship:

$$T_{ON,MAX} = (0.80 - I_{DROOP} \cdot 3.8k) \cdot T_{SW} = \begin{cases} 0.80 \cdot T_{SW} & I_{DROOP} = 0\mu A \\ 0.40 \cdot T_{SW} & I_{DROOP} = 105\mu A \end{cases}$$

Where I_{OUT} is the output current ($I_{OUT} = \Sigma \cdot I_{PHASEx}$) and T_{SW} is the switching period ($T_{SW} = 1/F_{SW}$).

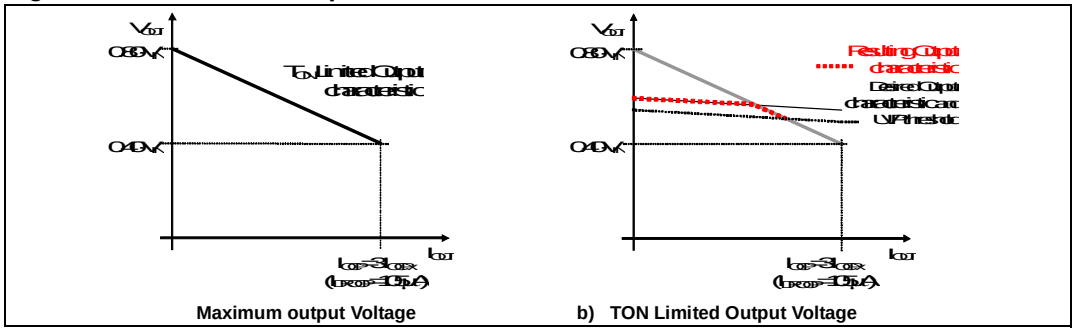
This linear dependence has a value at zero load of $0.80 \cdot T_{SW}$ and at maximum current of $0.40 \cdot T_{SW}$ typical and results in two different over current behaviors of the device:

14.5.1 T_{ON} Limited output voltage.

This happens when the maximum ON time is reached before that the current in each phase reaches IO_{CPx} ($I_{INFOx} < I_{OCTH}$). *Figure 17* shows the maximum output voltage that the device is able to regulate considering the T_{ON} limitation imposed by the previous relationship. If the desired output characteristic crosses the T_{ON} limited maximum output voltage, the output resulting voltage will start to drop after the crossing.

In this case, the device doesn't perform constant current limitation but only limits the maximum ON time following the previous relationship. The output voltage starts to decrease follows the resulting characteristic (dotted in *Figure 17*) until UVP is detected or anyway until I_{DROOP} =105µA.

Figure 17. TON limited operation



14.5.2 Constant current operation

This happens when the on-time limitation is reached after the valley current in each phase reaches I_{OCPx} ($I_{INFOx} > I_{OCTH}$).

The device enters in Quasi-Constant-Current operation: the low-side mosfets stays ON until the current read becomes lower than I_{OCPx} ($I_{INFOx} < I_{OCTH}$) skipping clock cycles. The high side mosfet can be then turned ON with a T_{ON} imposed by the control loop after the LS turn-off and the device works in the usual way until another OCP event is detected.

This means that the average current delivered can slightly increase in Quasi-Constant-Current operation since the current ripple increases. In fact, the ON time increases due to the OFF time rise because of the current has to reach the I_{OCPx} bottom. The worst-case condition is when the ON time reaches its maximum value.

When this happens, the device works in Constant Current and the output voltage decrease as the load increase. Crossing the UVP threshold causes the device to latch driving high the OSC pin (*Figure 18* shows this working condition).

It can be observed that the peak current (Ipeak) is greater than I_{OCPx} but it can be determined as follow:

$$I_{PEAK} = I_{OCPx} + \frac{V_{IN} - Vout_{MIN}}{L} \cdot Ton_{MAX} = I_{OCPx} + \frac{V_{IN} - Vout_{MIN}}{L} \cdot 0.40 \cdot T_{SW}$$

Where $Vout_{MIN}$ is the UVP threshold, (inductor saturation must be considered). When that threshold is crossed, all mosfets are turned off, the FAULT pin is driven high and the device stops working. Cycle the power supply or the OUTEN pin to restart operation.

The maximum average current during the Constant-Current behavior results:

$$I_{MAX,TOT} = 3 \cdot I_{MAX} = 3 \cdot \left(I_{OCPx} + \frac{Ipeak - I_{OCPx}}{2} \right)$$

In this particular situation, the switching frequency for each phase results reduced. The ON time is the maximum allowed (T_{onMAX}) while the OFF time depends on the application:

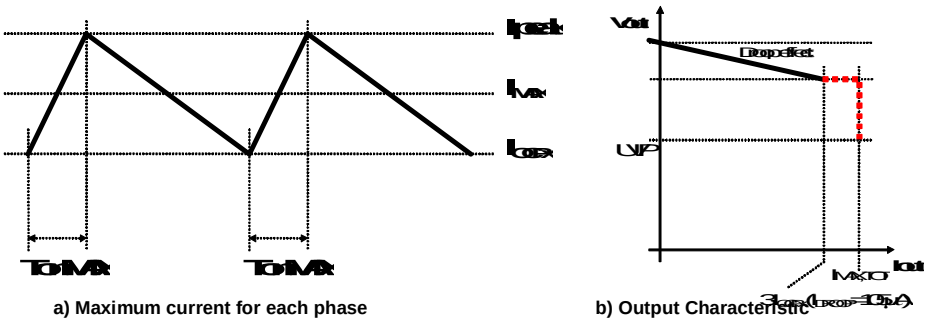
$$T_{OFF} = L \cdot \frac{Ipeak - I_{OCPx}}{V_{out}} \qquad F = \frac{1}{T_{onMax} + T_{OFF}}$$

The transconductance resistor Rg can be designed considering that the device limits the bottom of the inductor current ripple and also considering the additional current delivered during the quasi-constant-current behavior as previously described in the worst case conditions.

Moreover, when designing D-VID compatible systems, the additional current due to the output filter charge during dynamic VID transitions must be considered.

$$Rg = \frac{I_{OCPx(max)} \cdot R_{SENSE(max)}}{I_{OCTH(min)}} \text{ where } I_{OCPx} = \frac{I_{OUT(OCP)}}{3} - \frac{\Delta I_{PP}}{2} + \frac{I_{D\text{-}VID}}{3}$$

Figure 18. Constant current operation



a) Maximum current for each phase

b) Output Characteristic

14.6 Inductor sense over current (CS_SEL = SGND)

The device detects an over current when the I_{INFOx} overcome the fixed threshold I_{OCTH}. Since the device always senses the current across the inductor, the I_{OCTH} crossing will happen during the HS conduction time: as a consequence of OCP detection, the device will turn OFF the HS mosfet and turns ON the LS mosfet of that phase until I_{INFOx} re-cross the threshold or until the next clock cycle. This implies that the device limits the peak of the inductor current.

In any case, the inductor current won't overcome the I_{OCPx} value and this will represent the maximum peak value to consider in the OC design.

The device works in Constant-Current, and the output voltage decreases as the load increase, until the output voltage reaches the UVP threshold. When this threshold is crossed, all mosfets are turned off, the FAULT pin is driven high and the device stops working. Cycle the power supply or the OUTEN pin to restart operation.

The transconductance resistor Rg can be designed considering that the device limits the inductor current ripple peak. Moreover, when designing D-VID systems, the additional current due to the output filter charge during dynamic VID transitions must be considered.

$$Rg = \frac{I_{OCPx(max)} \cdot R_{SENSE(max)}}{I_{OCTH(min)}} \text{ where } I_{OCPx} = \frac{I_{OUT(OCP)}}{3} + \frac{\Delta I_{PP}}{2} + \frac{I_{D\text{-}VID}}{3}$$

15 Oscillator

The internal oscillator generates the triangular waveform for the PWM charging and discharging with a constant current an internal capacitor. The switching frequency for each channel, F_{SW}, is internally fixed at 150kHz so that the resulting switching frequency at the load side results in being tripled.

The current delivered to the oscillator is typically 25µA (corresponding to the free running frequency Fsw=150kHz) and it may be varied using an external resistor (R_{OSC}) connected between the OSC pin and SGND or VCC (or a fixed voltage greater than 1.24V). Since the OSC pin is fixed at 1.24V, the frequency is varied proportionally to the current sunk (forced) from (into) the pin considering the internal gain of 6KHz/µA.

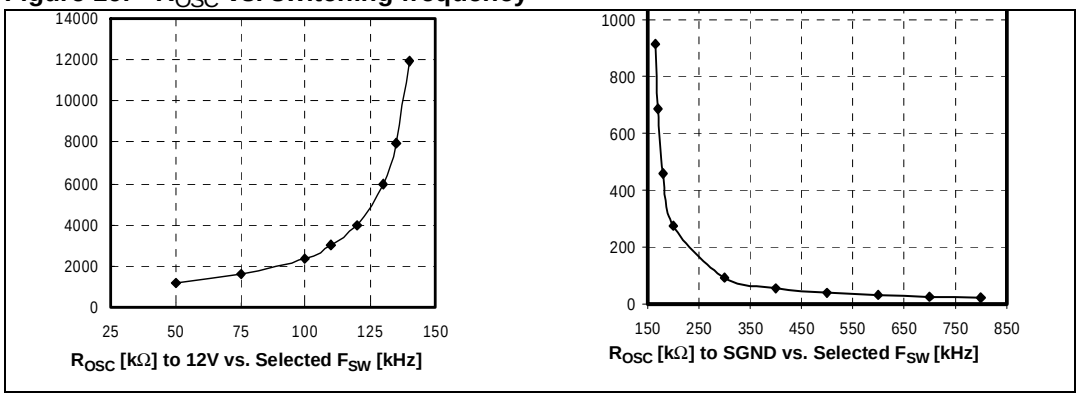
In particular connecting R_{OSC} to SGND the frequency is increased (current is sunk from the pin), while connecting R_{OSC} to VCC=12V the frequency is reduced (current is forced into the pin), according to the following relationships:

$$R_{OSC} \text{ vs. GND: } F_{SW} = 150kHz + \frac{1.237}{R_{OSC}(k\Omega)} \cdot 6\frac{kHz}{\mu A} = 150kHz + \frac{7.422 \cdot 10^6}{R_{OSC}(k\Omega)}$$

$$R_{OSC} \text{ vs. 12V: } F_{SW} = 150kHz + \frac{12\text{-}1.237}{R_{OSC}(k\Omega)} \cdot 6\frac{kHz}{\mu A} = 150kHz + \frac{6.457 \cdot 10^7}{R_{OSC}(k\Omega)}$$

Maximum programmable switching frequency depends on the Current Reading Method selected. When reading across LS mosfet, the maximum switching frequency per phase must be limited to 500kHz to avoid current reading errors causing, as a consequence, current sharing errors. When reading across the inductor, higher switching frequency can be approached (device power dissipation must be checked prior to design high switching frequency systems).

Figure 19. R_{OSC} vs. switching frequency



16 Driver section

The integrated high-current drivers allow using different types of power MOS (also multiple MOS to reduce the equivalent R_{dsON}), maintaining fast switching transition.

The drivers for the high-side mosfets use BOOTx pins for supply and PHASEx pins for return. The drivers for the low-side mosfets use VCCDRx pin for supply and PGNDx pin for return. A minimum voltage of 4.6V at VCCDRx pin is required to start operations of the device. VCCDRx pins must be connected together.

The controller embodies a sophisticated anti-shoot-through system to minimize low side body diode conduction time maintaining good efficiency saving the use of Schottky diodes: when the high-side mosfet turns off, the voltage on its source begins to fall; when the voltage reaches 2V, the low-side mosfet gate drive is suddenly applied. When the low-side mosfet turns off, the voltage at LGATEx pin is sensed. When it drops below 1V, the high-side mosfet gate drive is suddenly applied.

If the current flowing in the inductor is negative, the source of high-side mosfet will never drop. To allow the turning on of the low-side mosfet even in this case, a watchdog controller is enabled: if the source of the high-side mosfet doesn't drop for more than 240ns, the low side mosfet is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

The BOOTx and VCCDRx pins are separated from IC's power supply (VCC pin) as well as signal ground (SGND pin) and power ground (PGNDx pin) in order to maximize the switching noise immunity. The separated supply for the different drivers gives high flexibility in mosfet choice, allowing the use of logic-level mosfet. Several combination of supply can be chosen to optimize performance and efficiency of the application.

Power conversion input is also flexible; 5V, 12V bus or any bus that allows the conversion (See maximum duty cycle limitations) can be chosen freely.

16.1 Power dissipation

Two main terms contribute in the device power dissipation: bias power and drivers' power. The first one depends on the static consumption of the device through the supply pins and it is simply quantifiable as follow:

$$P_{DC} = V_{CC} \cdot (I_{CC} + 3 \cdot I_{CCDRx} + 3 \cdot I_{BOOTx})$$

Drivers' power is the power needed by the driver to continuously switch on and off the external mosfets; it is a function of the switching frequency and total gate charge of the selected mosfets. It can be quantified considering that the total power P_{SW} dissipated to switch the mosfets (easy calculable) is dissipated by three main factors: external gate resistance (when present), intrinsic mosfet resistance and intrinsic driver resistance. This last term is the important one to be determined to calculate the device power dissipation.

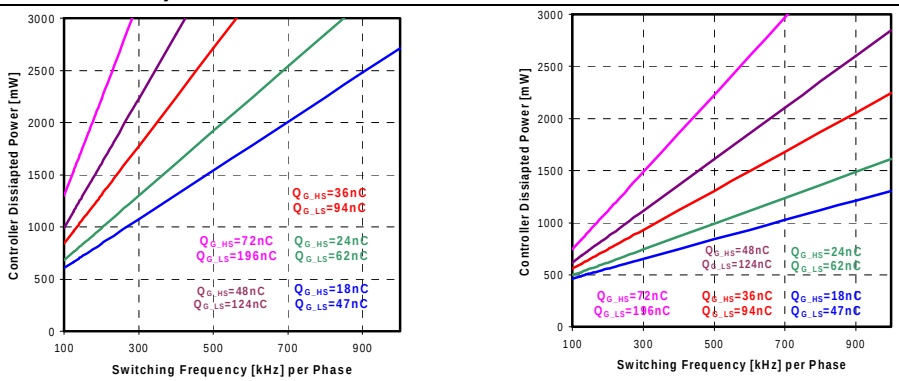
The total power dissipated to switch the mosfets results:

$$P_{SW} = 3 \cdot (Q_{G\_HS} \cdot V_{BOOT} + Q_{G\_LS} \cdot V_{CCDR}) \cdot F_{SW}$$

External gate resistors helps the device to dissipate the switching power since the same power P_{SW} will be shared between the internal driver impedance and the external resistor resulting in a general cooling of the device.It is important to determine the device dissipated power in order to avoid the junction working beyond its maximum operative temperature.

Moreover, since the device has an exposed pad to better dissipate the power, also the thermal resistance between junction and ambient is important.
Figure 16 shows the Switching Power for different kind of mosfets driven.

Figure 20. Controller power dissipated (Quiescent + Switching; $V_{CC} = V_{CCDR} = V_{BOOT}$ = 12V)

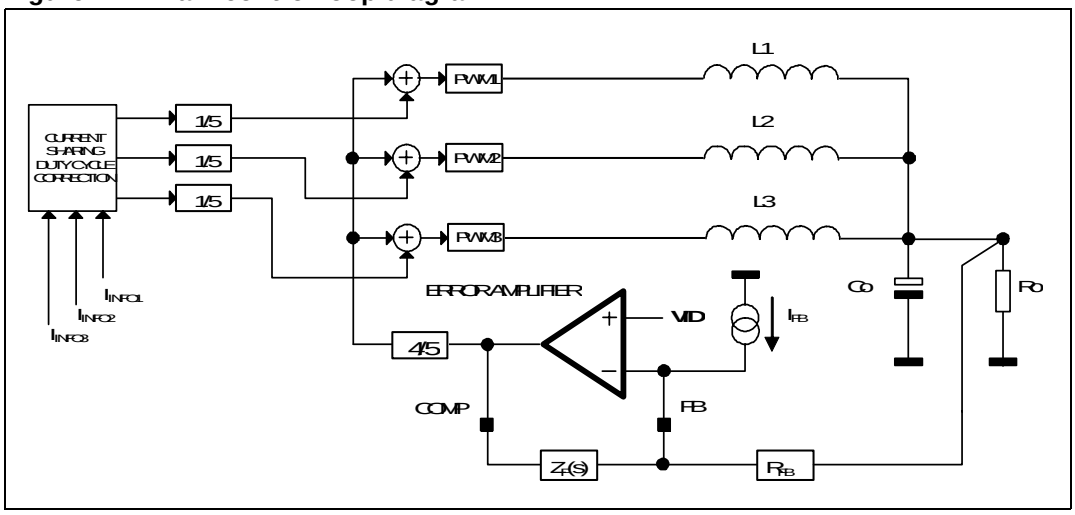


$R_{GATE} = R_{GATE\_MOSFET} = 0$ $R_{GATE\_HS} = 2.2\Omega$; $R_{GATE\_LS} = 3.3\Omega$; · $R_{GATE\_MOSFET} = 1\Omega$

17 System control loop compensation

The control loop is composed by the Current Sharing control loop and the Average Current Mode control loop. Each loop gives, with a proper gain, the correction to the PWM in order to minimize the error in its regulation: the Current Sharing control loop equalize the currents in the inductors while the Average Current Mode control loop fixes the output voltage equal to the reference programmed by VID. *Figure 21* shows the block diagram of the system control loop.

Figure 21. Main control loop diagram



The average current mode control loop is reported in *Figure 22*. The current information I_{FB} sourced by the FB pin flows into R_{FB} implementing the dependence of the output voltage from the read current.

The system can be modeled with an equivalent single phase converter which only difference is the equivalent inductor L/3 (where each phase has an L inductor).The ACM control loop gain results (obtained opening the loop after the COMP pin):

$$G_{LOOP}(s) = -\frac{PWM \cdot Z_F(s) \cdot (R_{DROOP} + Z_P(s))}{(Z_P(s) + Z_L(s)) \cdot \left[\frac{Z_F(s)}{A(s)} + \left(1 + \frac{1}{A(s)}\right) \cdot R_{FB}\right]}$$

Where:

- R_{SENSE} is the mosfet R_{dsON} or the Inductor DCR depending on the sensing element selected;
- $R_{DROOP} = \frac{R_{SENSE}}{Rg} \cdot R_{FB}$ is the equivalent output resistance determined by droop;
- $Z_P(s)$ is the impedance resulting by the parallel of the output capacitor (and its ESR) and the applied load Ro;
- $Z_F(s)$ is the compensation network impedance;
- $Z_L(s)$ is the parallel of the three inductor impedance;
- A(s) is the error amplifier gain;

- $PWM = \frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{osc}}$ is the PWM transfer function where ΔV_{OSC} is the oscillator ramp amplitude and has a typical value of 3V

Removing the dependence from the Error Amplifier gain, so assuming this gain high enough, the control loop gain results:

$$G_{LOOP}(s) = -\frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{Z_F(s)}{Z_P(s) + Z_L(s)} \cdot \left(\frac{Rs}{Rg} + \frac{Z_P(s)}{R_{FB}}\right)$$

With further simplifications, it results:

$$G_{LOOP}(s) = -\frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{Z_F(s)}{R_{FB}} \cdot \frac{Ro + R_{DROOP}}{Ro + \frac{R_L}{3}} \frac{1 + s \cdot Co \cdot (R_{DROOP} // Ro + ESR)}{s^2 \cdot Co \cdot \frac{L}{3} + s \cdot \left[\frac{L}{3 \cdot Ro} + Co \cdot ESR + Co \cdot \frac{R_L}{3}\right] + 1}$$

Considering now that in the application of interest it can be assumed that $Ro >> R_L$; $ESR << Ro$ and $R_{DROOP} << Ro$, it results:

$$G_{LOOP}(s) = -\frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{Z_F(s)}{R_{FB}} \cdot \frac{1 + s \cdot Co \cdot (R_{DROOP} + ESR)}{s^2 \cdot Co \cdot \frac{L}{3} + s \cdot \left[\frac{L}{3 \cdot Ro} + Co \cdot ESR + Co \cdot \frac{R_L}{3}\right] + 1}$$

The ACM control loop gain is designed to obtain a high DC gain to minimize static error and cross the 0dB axes with a constant -20dB/dec slope with the desired crossover frequency ω_T. Neglecting the effect of $Z_F(s)$, the transfer function has one zero and two poles.

Both the poles are fixed once the output filter is designed and the zero is fixed by ESR and the Droop resistance.

To obtain the desired shape an R_F-C_F series network is considered for the $Z_F(s)$ implementation. A zero at $\omega_F = 1/R_F C_F$ is then introduced together with an integrator. This integrator minimizes the static error while placing the zero in correspondence with the L-C resonance a simple -20dB/dec shape of the gain is assured).

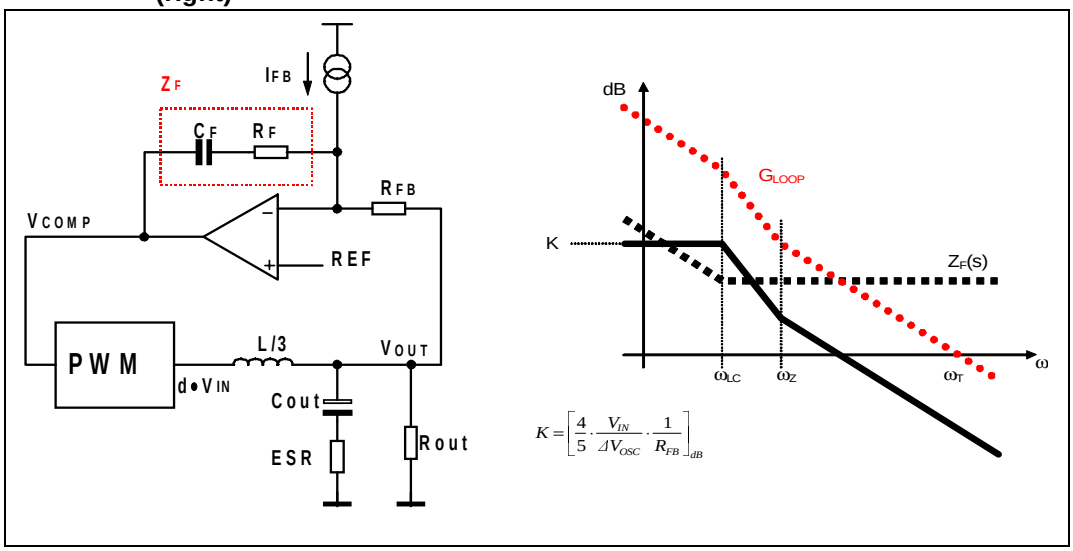
In fact, considering the usual value for the output filter, the LC resonance results to be at frequency lower than the above reported zero.

Compensation network can be simply designed placing $\omega_Z = \omega_{LC}$ and imposing the cross-over frequency ω_T as desired obtaining:

$$R_F = \frac{R_{FB} \cdot \Delta V_{OSC}}{V_{IN}} \cdot \frac{5}{4} \cdot \omega_T \cdot \frac{L}{3 \cdot (R_{DROOP} + ESR)}$$

$$C_F = \frac{\sqrt{Co \cdot \frac{L}{3}}}{R_F}$$

Figure 22. Equivalent Control Loop Gain Block Diagram (left) and Bode Diagram (right)



18 Layout guidelines

Since the device manages control functions and high-current drivers, layout is one of the most important things to consider when designing such high current applications.

A good layout solution can generate a benefit in lowering power dissipation on the power paths, reducing radiation and a proper connection between signal and power ground can optimize the performance of the control loops.

Integrated power drivers reduce components count and interconnections between control functions and drivers, reducing the board space.

Here below are listed the main points to focus on when starting a new layout and rules are suggested for a correct implementation.

18.1 Power connections.

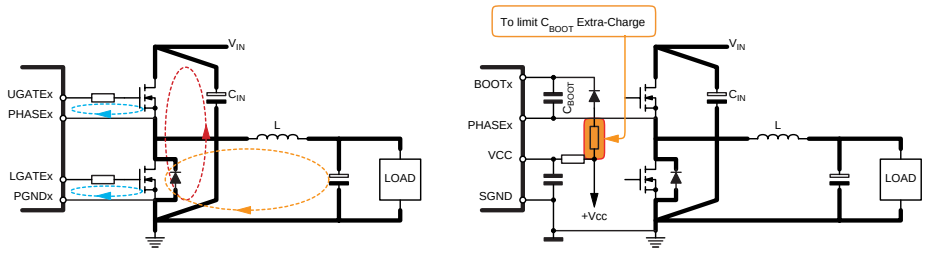
These are the connections where switching and continuous current flows from the input supply towards the load. The first priority when placing components has to be reserved to this power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (EMI and losses) these interconnections must be a part of a power plane and anyway realized by wide and thick copper traces: loop must be anyway minimized. The critical components, i.e. the power transistors, must be located as close as possible one to the other.

Figure 23 shows the details of the power connections involved and the current loops. The input capacitance (C_{IN}), or at least a portion of the total capacitance needed, has to be placed close to the power section in order to eliminate the stray inductance generated by the copper traces. Low ESR and ESL capacitors are preferred.

Use as much VIAs as possible when power traces have to move between different planes on the PCB: this reduces both parasitic resistance and inductance. Moreover, reproducing the same high-current trace on more than one PCB layer will reduce the parasitic resistance associated to that connection.

Connect output bulk capacitor as near as possible to the load, minimizing parasitic inductance and resistance associated to the copper trace also adding extra decoupling capacitors along the way to the load when this results in being far from the bulk capacitor bank.

Figure 23. Power connections and related connections layout guidelines (same for all phases).



a. PCB power and ground planes areas

b. PCB small signal components placement

18.2 Power connections related.

Figure 24 shows some small signal components placement.

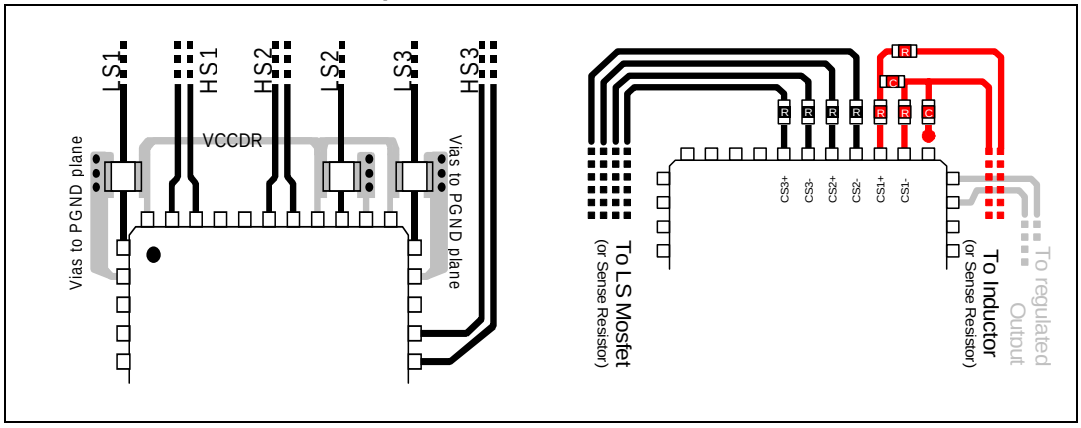
- *Gate and phase traces* must be sized according to the driver RMS current delivered to the power mosfet. The device robustness allows managing applications with the power section far from the controller without losing performances. Anyway, when possible, it is suggested to minimize the distance between controller and power section.
  In addition, since the PHASEx pin is the return path for the high side driver, this pin might be connected directly to the High Side mosfet Source pin to have a proper driving for this mosfet. For the LS mosfets, the return path is the PGNDx pin: it can be connected directly to the power ground plane.
- *Bootstrap capacitor* must be placed as close as possible to the BOOTx and PHASEx pins to minimize the loop that is created.
- *Decoupling capacitor from* VCC and SGND placed as close as possible to the involved pins.
- *Decoupling capacitor from* VCCDRx and PGNDx placed as close as possible to those pins. This capacitor sustains the peak currents requested by the low-side mosfet drivers.
- *Sensible components* must be referred to SGND (when present): frequency set-up resistor R_{OSC}, offset resistor R_{OFFSET}, TC resistor R_{TC} and OVP resistor R_{OVP}.
- *Star grounding:* Connect SGND to PGND plane in a single point to avoid that drops due to the high current delivered causes errors in the device behavior.
- An additional ceramic capacitor is suggested to place near HS mosfet drain. This helps in reducing HF noise.
- VSEN pin filtered vs. SGND helps in reducing noise injection into device.
- OUTEN pin filtered vs. SGND helps in reducing false trip due to coupled noise: take care in routing driving net for this pin in order to minimize coupled noise.
- *PHASE pin spikes*. Since the HS mosfet switches hardly, heavy voltage spikes can be observed on the PHASEx pins. If these voltage spikes overcome the max breakdown voltage of the pin, the device can absorb energy and it can cause damages. The voltage spikes must be limited by proper layout; by the use of gate resistors, Schottky diodes in parallel to the low side mosfets and/or snubber network on the low side mosfets, and cannot overcome 26V, for 20nSec, at F_{SW} = 600kHz.
- *Boot Capacitor Extra Charge.* Systems that do not use Schottky diodes might show big negative spikes on the phase pin. This spike can be limited as well as the positive spike but has an additional consequence: it causes the bootstrap capacitor to be over-charged. This extra-charge can cause, in the worst case condition of maximum input voltage and during particular transients, that boot-to-phase voltage overcomes the abs. max. ratings also causing device failures. It is then suggested in this cases to limit this extra-charge by adding a small resistor in series to the boot diode (one resistor can be enough for all the three diodes if placed upstream the diode anode, see *Figure 23*).

18.3 Current sense connections.

Remote Buffer: The input connections for this component must be routed as parallel nets from the FBG/FBR pins to the load in order to compensate losses along the output power traces and also to avoid the pick-up of any common mode noise. Connecting these pins in points far from the load will cause a non-optimum load regulation, increasing output tolerance.

Current Reading: The Rg resistors have to be placed as close as possible to the CSx- and CSx+ pins in order to limit the noise injection into the device; this is still valid also for the $R_{g(RC)}$-Cg network used when sensing current across the inductor. The PCB traces connecting these resistors to the reading point must use dedicated nets, routed as parallel traces in order to avoid the pick-up of any common mode noise.

Figure 24. Device orientation (left) and sense nets routing (right: red for Lsense, black for LSsense)



It's also important to avoid any offset in the measurement and, to get a better precision, to connect the traces as close as possible to the sensing elements. Symmetrical layout is also suggested.

Small filtering capacitor can be needed between VOUT and SGND on the CSx- line, placed near the controller, allowing higher layout flexibility in the current sense connection.

19 Embedding L6711-based VRDs...

When embedding the VRD into the application, additional care must be taken since the whole VRD is a switching DC/DC regulator and the most common system in which it has to work is a digital system such as MB or similar. In fact, latest MB has become faster and powerful: high speed data bus are more and more common and switching-induced noise produced by the VRD can affect data integrity if not following additional layout guidelines. Few easy points must be considered mainly when routing traces in which switching high currents flow (switching high currents cause voltage spikes across the stray inductance of the traces causing noise that can affect the near traces):

Keep safe guarding distance between high current switching VRD traces and data buses, especially if high-speed data bus to minimize noise coupling.

Keep safe guard distance or filter properly when routing bias traces for I/O sub-systems that must walk near the VRD.

Possible causes of noise can be located in the PHASE connections, Mosfet gate drive and Input voltage path (from input bulk capacitors and HS drain). Also PGND connections must be considered if not insisting on a power ground plane. These connections must be carefully kept far away from noise-sensitive data bus.

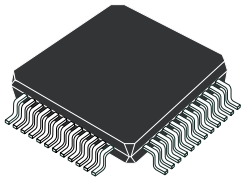
Since the generated noise is mainly due to the switching activity of the VRM, noise emissions depend on how fast the current switch. To reduce noise emission levels, it is also possible, in addition to the previous guidelines, to reduce the current slope and then to increase the switching times: this will cause, as a consequence of the higher switching time, an increase in switching losses that must be considered in the thermal design of the system.

20 TQFP48 Mechanical data & package dimensions

Figure 25. TQFP48 Mechanical data & package dimensions

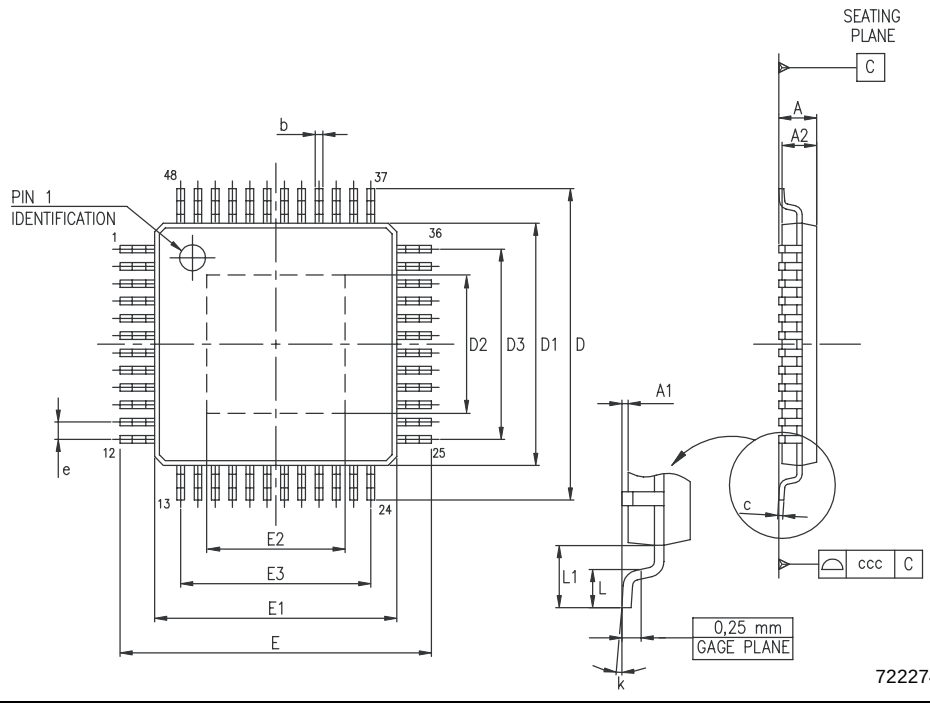
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.006	0.008	0.010
c	0.09		0.20	0.004		0.008
D	8.80	9.00	9.20	0.346	0.354	0.362
D1	6.80	7.00	7.20	0.268	0.276	0.283
D2	2.00		4.25	0.079		0.167
D3		5.50			0.217	
e		0.50			0.020	
E	8.80	9.00	9.20	0.346	0.354	0.362
E1	6.80	7.00	7.20	0.268	0.276	0.283
E2	2.00		4.25	0.079		0.167
E3		5.50			0.217	
e		0.50			0.019	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°(min.), 3.5°(typ.), 7°(max.)					
ccc			0.08			0.0031

OUTLINE AND MECHANICAL DATA



Body: 7 x 7 x 1.0mm

TQFP48 - EXPOSED PAD



21 Revision history

Table 8. Revision History

Date	Revision	Changes
01-Jun-2004	1	First Issue
23-Nov-2004	2	Modificated the Paragraph 18.2 on the page 32/38.
26-Oct-2005	3	Added new paragraph 9.1.2 Warning 2.
18-Apr-2006	4	Updated graphic, Modified Table1

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZE REPRESENTATIVE OF ST, ST PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS, WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com